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Low-density parity-check code for high-speed fibre-optic communication and its experimental verification

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Abstract: Although low-density parity-check (LDPC) code has been proved as a powerful forward error correction code for fibre optic communication, its soft-decoding requires high quantisation resolution which is difficult to achieve for high-speed fibre-optic communication systems. A modification to LDPC decoding algorithms is proposed to effectively improve the performance at quantisation resolution as low as two-bit or one-bit. The good decoding performance of LDPC code for error correction is confirmed by experiment. Compared with the RS(255, 239) code commonly used in optical fibre communication, a Q-factor improvement of 2-dB is obtained in the experiment for an LDPC code with quasi-cyclic structure at the same redundancy as the RS code. Furthermore, the impacts of sampling phase and channel estimation using real data over the decoding performance are analysed.

1 Introduction

Error correction codes have been considered to be one of the key technologies for future wavelength division multiplexing fibre-optic communication systems with high data rate and large total capacity. The most commonly used forward error correction (FEC) scheme in present fibre-optic communication systems is Reed–Solomon (RS) code, especially the RS(255, 239) code as defined in ITU-T recommendation G.975 [1]. Several super-FEC codes have been studied in the ITU-T recommendation G.975.1 with better performances than the RS(255, 239) code [2]. But these super-FEC codes usually have higher redundancies or much longer code length.

Vasic and Djordjevic first proposed to use low-density parity-check (LDPC) code for high-speed fibre-optic communication systems in [3]. Through extensive computer simulation, they found that the LDPC code can achieve a better performance than the RS(255, 239) code at a similar redundancy with soft decoding. Inspired by this result, they later studied different LDPC codes constructed using combinatorial design at different redundancies for different coding gains [4–8]. Other than computer simulations, it has been experimentally verified that under fibre polarisation mode dispersion effects, the LDPC codes can achieve considerable performance gain together with turbo equalisation [9, 10].

However, compared with the RS(255, 239) code with hard decoding in the present systems, soft decoding of LDPC codes is required in order to achieve such a benefit. Unfortunately, analogue-to-digital conversion (ADC) with high quantisation resolution for soft decoding of LDPC codes is not available for 10 Gbps or higher speed fibre-optic communication systems. The ADCs at 10 Gbps used in several recent experiments for maximum-likelihood sequence estimation (MLSE)-based electrical dispersion compensation (EDC) [11] or soft decoding of block turbo code [12] have a quantisation resolution of three bits only. In this paper, we show that a modification to the original LDPC min-sum (MS) decoding algorithm can help to improve the decoding performance at low quantisation resolution.

We also demonstrate our experimental verification on the decoding performance of the LDPC code. Unlike computer simulation and the previous experimental studies, this paper aims to study how the LDPC code performance is affected by implementation issues like signal sampling phases and so on, where performance fluctuation because of different sampling phases and optical signal power fluctuation is observed from the experimental results.

The rest of this paper is organised as follows. Section 2 gives a brief introduction of the LDPC code used in this paper and the modified decoding algorithm. In Section 3, the experimental set-up for this study is introduced, followed by detailed analysis on the experimental results. Section 4 discusses about several hardware implementation issues at the high speed required for fibre-optic communications systems. Finally, Section 5 concludes the paper.

2 LDPC code and the modified decoding algorithm

The LDPC code used in this paper has a redundancy of 6.67%, similar to the RS(255, 239) code. Its parity check matrix $\boldsymbol{H}$ is defined in (1) as

$$\boldsymbol{H} = [\boldsymbol{H}_1 \quad \boldsymbol{H}_2 \quad \dots \quad \boldsymbol{H}_{16}] \tag{1}$$

where $\boldsymbol{H}_1 - \boldsymbol{H}_{16}$ are 16 circulant matrices of size 255 × 255. Each one of them has a column or row weight of 4 or 5. The location of '1' in the circulant matrix is generated randomly with a requirement that cycle 4 is avoided. Compared with those LDPC codes of similar redundancies from the references, our quasi-cyclic LDPC (QC-LDPC) code shows a slightly worse performance. For example, the best LDPC code from the references is a 5.3% redundancy LDPC (2461, 2338) code which has a coding gain of 2.1 dB over RS(255, 239) code at a bit error rate (BER) of 10^{-8} [3]. Compared with this result, our chosen QC-LDPC code with a redundancy of 6.67% has a coding gain of 2 dB over RS(255, 239) code at 10^{-8}. However, we believe that the quasi-cyclic structure in our code can benefit in encoder/decoder implementation at the high data rates required for fibre-optic communications. As will be discussed in Section 4, the quasi-cyclic structure allows implementation of the encoder with shift registers, and it also helps in the memory allocation and memory access in an orderly way for the information exchange during decoding.

For LDPC decoding, the belief propagation (BP) algorithm can be used and its row and column operations are defined in (2) and (3) separately

$$R_{j,m} = 2\tanh^{-1}\left(\prod_{m' \in M(j)\backslash j} \tanh(Q_{j,m'}/2)\right) \tag{2}$$

$$Q_{j,m} = L_m + \sum_{j' \in J(m)\backslash j} R_{j',m} \tag{3}$$

where $Q_{j,m}$ and $R_{j,m}$ are the log-likelihood ratio (LLR) for the variable nodes and the check nodes, respectively, and L_m is the LLR from initialisation. The MS algorithm approximates (2) with

$$R_{j,m} \simeq \min_{m' \in M(j)\backslash m} |Q_{j,m'}| \prod_{m' \in M(j)\backslash m} \mathrm{sgn}(Q_{j,m'}) \tag{4}$$

and it allows a much easier implementation for decoding at some performance cost.

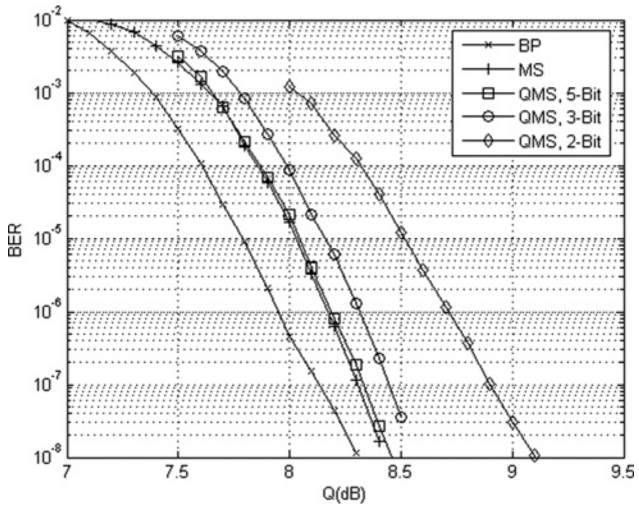

Figure 1 *Quantisation effect on decoding LDPC code*
'QMS' means MS decoding with quantisation

We have tried the BER performance of the MS decoding algorithm with several different quantisation resolutions including 2-bit, 3-bit and 5-bit quantisation and without quantisation using simulation. The simulation results are compared in Fig. 1 for a fibre-optic communication system with the conventional on–off keying modulation. It is clear that 3-bit quantisation is enough for the performance loss to be within 0.1 dB. Unfortunately, when the available quantisation resolution is below 3-bit, the decoding performance deteriorates significantly.

It has been shown that some simple modification to the MS decoding algorithm can be used to reduce the performance gap between the MS and the BP algorithms [13]. Instead of modifying (4) as in the reference, this paper modifies (3) to

$$Q_{j,m} = \alpha\left[L_m + \sum_{j' \in J(m)\backslash j} R_{j',m}\right] \tag{5}$$

where α is a constant factor optimised through simulation and we call this modified decoding algorithm min-sum factorisation (MSF) decoding. Although similar, the above (5) is not identical to equation (15) in [13], where the local information is not included in the modification. Simulation results with MSF decoding for 2-bit or 1-bit quantisation are shown in Fig. 2. For 2-bit quantisation, with 0.6 dB performance improvement from the modification, the decoding

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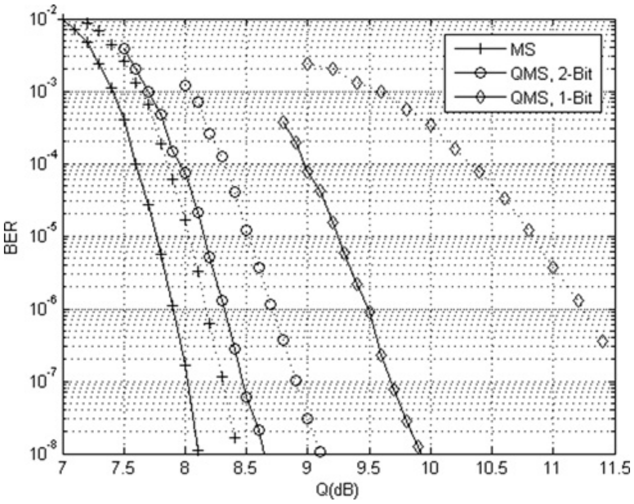

Figure 2 *Performance comparisons between decoding algorithms with modification (solid lines) and without modification (dash lines)*

performance is within 0.2 dB for the MS decoding without quantisation. For 1-bit quantisation, the performance gain from the modification can be as high as 2 dB. The MS decoding without quantisation can also benefit from the modification with about 0.3 dB performance gain. Another algebraically generated LDPC code with different redundancy is also tested with MSF decoding and similar performance improvement can also be achieved.

3 Experimental verification

Fig. 3 depicts the schematic of our experimental set-up for testing the decoding performance of the selected LDPC codes. A sequence of 3825 random data bits is first generated and encoded using MATLAB to obtain a pre-coded test pattern C. The code C is then saved in the pulse pattern generator (PPG) for the following experiment. Computer simulation results confirm that there is no performance difference between the fixed randomly generated code and full random codes. The output from the PPG is used to modulate the laser diode at a bit rate of 2 Gbit/s with a non-return-to-zero (NRZ) pulse shape.

Since we are focusing on the decoding performance of the LDPC code, fibre transmission effects, like dispersion, fibre non-linearity, and so on, are not included and a back-to-back system is used for the experiment. A variable optical attenuator is used to set the received optical power to the desired value for the PIN diode and trans-impedance amplifier (PIN + TIA) receiver. After O/E conversion, the signal is sampled using a digital oscilloscope at 10 Gsamples/s, five times the bit rate, and each recorded data sample is of 8-bit quantisation resolution. The five times over-sampling makes it possible to study samples from different sampling phases later and the bit rate is thus limited to 2 Gbit/s. Since no optical amplifier is present in the system, the dominant noise in the received signal comes from the electrical amplifier after O/E conversion. The saved data samples are then processed and decoded offline with a personal computer using MATLAB.

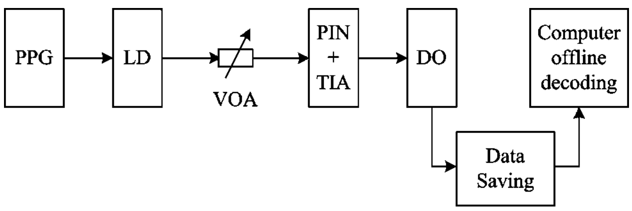

Figure 3 *Experimental set-up*

PPG: pulse-pattern generator; LD: laser-diode; VOA: variable optical attenuator; PIN + TIA: PIN diode and trans-impedance amplifier; DO: digital oscilloscope

Before decoding, timing synchronisation, frame synchronisation and channel estimation have to be done using the saved data samples and these processes are repeated for each saved data block.

1. *Timing synchronisation:* Timing synchronisation is usually obtained with a clock recovery (CR) block in the optical receiver to determine the best sampling phase of the signal for soft decoding. Since CR is not included in our PIN + TIA receiver, timing synchronisation has to be obtained using the saved data samples. From the recorded five samples per bit, the effect of the sampling phases on the decoding performance can be studied and the results are discussed later.

2. *Frame synchronisation:* For a linear block code like the studied LDPC code, frame synchronisation is necessary for decoding. Here, we use the pre-coded test pattern for frame synchronisation.

3. *Channel estimation:* Since optical amplifiers are not present in the experiment, the dominant noise is that from electrical amplifiers in the receiver and the data samples are thus of Gaussian distribution. The mean and standard deviation of bit '1' and '0' should be determined for the soft decoding of the LDPC codes. Unlike computer simulation where they are known, here the mean and standard deviation are computed using the saved data samples for each data frame. *Q*-factor fluctuation on the order of 0.15 dB from frame to frame is observed in the experiment even for a fixed optical attenuation. For comparison, computer simulation results show that a 0.2 dB increase in the *Q*-factor can reduce the BER by an order of magnitude with the studied LDPC code.

Fig. 4 compares the experimental results and the simulation results for the performance of the selected LDPC code. The 2-dB coding gain of LDPC code over RS(255, 239) code in the simulation is confirmed by the experiment. Note that in the simulations, the mean and the standard deviation of the received signal are known in advance and they are fixed through the simulation for a fixed *Q*-factor. However, in the experiment, channel parameters like the mean and the

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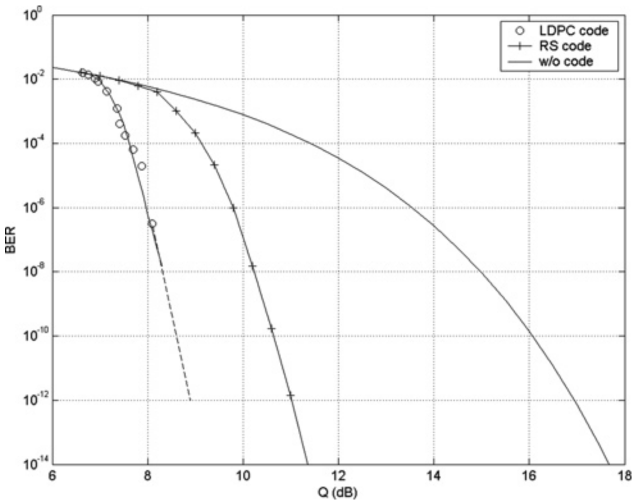

Figure 4 *BER comparison between LDPC code and RS code*

For the LDPC code, the solid line is simulation results, the scattered points are experimental results and the dashed line is extrapolated from simulation for comparison with RS code

standard deviation for each data frame are found based on a frame-by-frame computation and then used in the decoding. A Q-factor fluctuation on the order of 0.15 dB for different frames can be observed and causes the BER performance in the experiment to be slightly worse than the BER performance in the simulation. The 0.2 dB performance loss with MS decoding is also confirmed from the experimental results.

The received signal has to be sampled at the correct phase for soft decoding of LDPC codes for better performance. For example, if the sampling phase is at the peak of the pulse, the highest Q-factor or signal-to-noise ratio is obtained; otherwise, the Q-factor is lowered and the decoding performance becomes worse. With a five times over-sampling rate on the received signal, decoding performances with samples from five different sampling phases are compared. For example, Fig. 5 shows the eye-plot

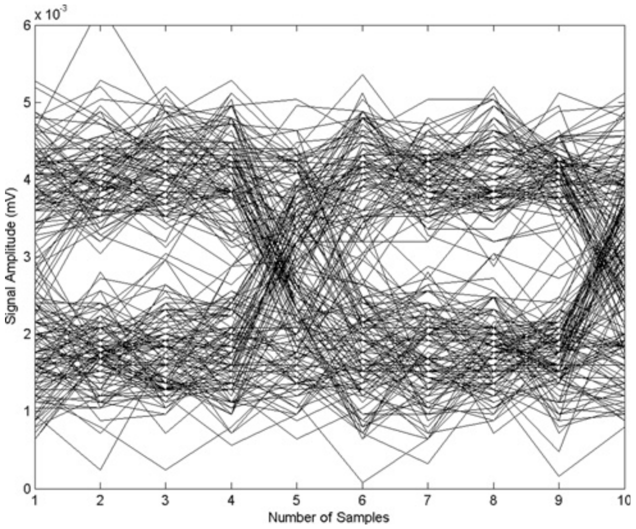

Figure 5 *Eye-plot of the experimental data*

for one fixed group of experimental data and the Q-factors obtained from three 'better' samples of this group of data are 7.41, 8.12 and 8.43 dB. A Q-factor fluctuation over 1 dB is observed and the BERs using these three sampling phases can differ by five orders of magnitude following the Q-factor difference. The other two sampling phases are believed to be on the side of the bit transition and have very low Q-factors. We believe that this Q-factor fluctuation comes from the non-ideal NRZ pulse shape from the laser transmitter in the experiment.

4 Discussion on hardware implementation

For practical application of LDPC codes in high-speed fibre-optic communication systems, we have to consider not only the performance gain, but also the high-speed hardware implementation issues. If one of the circulant matrices in the parity-check matrix from (1) is invertible, the corresponding generator matrix for the LDPC code is also circulant and the encoder can be implemented using shift registers for such a generator matrix composed of circulant matrices.

However, the hardware implementation of the decoder is much more difficult for the following reasons. First, the BP-decoding algorithm requires very complicated mathematical computation for its row operations as shown in (2). Consequently, the MS-decoding is preferred because of its simplicity for high-speed implementation. The performance loss can be removed using the modified decoding algorithm studied in Section 2.

Secondly, soft decoding of LDPC codes requires sampling the signal at a high speed for fibre-optic communication systems at 10 Gbps or higher bit rates. The modification to the original MS-decoding algorithm from Section 2 can be used to ease the problem.

Thirdly, the LLR information for the check nodes and the variable nodes has to be stored and exchanged during the iterative LDPC decoding process. If each piece of LLR information is represented using 8-bits, a memory of about 40 K bytes in total is required. Even though a memory of this size is not a problem, the problem lies in the memory access. For example, each row of the parity-check matrix $\boldsymbol{H}$ used in this paper has 70 '1's, thus the 70 LLR values have to be taken out from the memory for the row operation. If the 70 LLR values are stored at one memory block, 70 clock periods must pass as only one memory unit can be accessed at one time. For high-speed implementation, the LLR values should be distributed in different memories to allow simultaneous access of the 70 memory units. Unlike an LDPC code with a randomly generated parity-check matrix, the QC-LDPC code can store the LLR values at 70 memory blocks, as shown in Fig. 6. With such a memory distribution, the 70 LLR values for any row operation are stored at 70 different memory blocks and thus can be accessed simultaneously.

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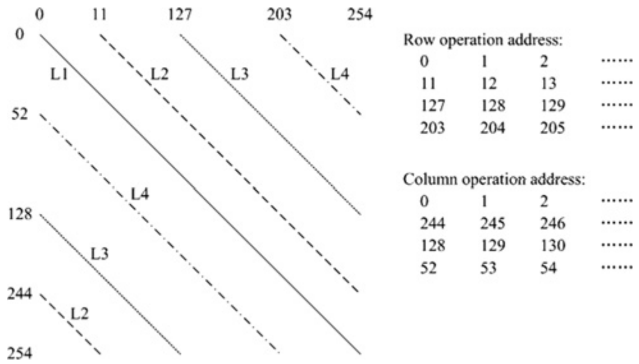

Figure 6 *Schematic of memory storage of LLR information for LDPC decoder*

There are 70 '1's on each line, and the corresponding 70 LLR values stored at different memory block

Similarly, for each column operation, the required LLR values are also stored at different memory blocks for possible simultaneous access. Moreover, the address for the memory access from row-to-row or column-to-column is put in an orderly way for easy implementation.

Fig. 6 shows one of the 16 circulant matrices from (1), where the row and column weight is 4. The four lines, L_1, L_2, L_3 and L_4, represent the locations of '1's in the matrix. According to our scheme, the LLR values for each one of the four lines are stored at one memory block. Thus, for the operation of the first row, the addresses for the four memory blocks are 0, 11, 127 and 203, respectively; for the operation of the second row, the addresses for the four memory blocks are 1, 12, 128 and 204, and so on. The column operations follow a similar order.

5 Conclusions

The effect of quantisation on the soft decoding of LDPC codes in fibre-optic communication systems is studied through simulation and the decoding performances for several quantisation resolutions are compared in this paper. It is found that low-bit quantisation may cause severe deterioration in the decoding performance. To improve the low-bit quantised soft decoding, a simple modification to the decoding algorithms is proposed. Simulation results show that the modified 2-bit quantised MS decoding can achieve about 0.6 dB performance gain compared to the case without modification. Moreover, the proposed modification scheme can also be applied to the BP and the MS decoding algorithms for a better performance.

The decoding performance of LDPC code is also verified by experiment where 2-dB coding gain over RS(255, 239) code can be obtained at the same redundancy with the quasi-cyclic LDPC code studied in the simulation. Even though *Q*-factor fluctuation cannot be avoided in the experiment, the experimental BER is only slightly worse than the one from the simulation. Unlike simulation studies where synchronisation and channel parameters are known, the experimental data are processed for timing synchronisation, frame synchronisation and channel estimation for each data frame before decoding in the experiment. Furthermore, the impact of sampling phase over decoding performance is analysed using five times over-sampling rate on the received signal. Over 1-dB *Q*-factor fluctuation from different sampling phases is possible even for the same group of experimental data.

Moreover, the proposed LDPC code has a quasi-cyclic structure which provides a way for distributed memory storage and access of LLR information during row and column operations of the information exchange in an orderly way. The encoder and decoder implementation of such a LDPC code can more easily meet the high-speed requirement for fibre-optic communication systems.

6 Acknowledgment

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