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A novel design of variable-rate RS encoder for ubiquitous high performance multimedia service in Gbps transmission system

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Abstract In this paper, we have first reviewed the state-of-the-art technologies related to DOCSIS 3.0 high-speed data transmission system and also looked at current trends in the next generation Gbps transmission technology, which is one of key technology for ubiquitous high performance multimedia service environments. Also, we implemented the RS encoder which was designed using VHDL and verified its operation in order to confirm our design through the ModelSim simulation analysis tool.

Keywords Channel bonding · Gbps transmission · RS encoder

1 Introduction

In the recent years, the advent of broadband convergence network (BcN) is essential for broadcasting/communication convergence along with digitalization trend for each broadcasting media. Development of access network connecting the user and BcN is the core area of technology for broadcasting/communication convergence. Giga-bps cable transceiver system based on HFC (Hybrid Fiber Coax) network emerges as a leading alternative of current access network (broadband high-speed network in charge of final 1 mile of BcN); it is because this network demonstrates excellent performance in terms of economic or technical aspects than FTTH (Fiber to the Home) or xDSL (Digital Subscriber Line).

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If using the 1 Gbps cable transceiver system based on the HFC network as an access network of broadband convergence network, it not only provides broadband high-speed data service to subscribers effectively, but also facilitates the implementation of XoD (Everything on Demand) using existing the digital cable broadcasting system. While experts agree that future broadcasting may converge into the form of XoD, its concrete implementation method has not been presented yet. However, the Gbps cable transceiver system has emerged as a realistic alternative for the implementation of XoD and the future broadcasting services [1–3].

Digital cable broadcasting can provide multimedia services including two-way additional services such as data broadcasting and VoD (Video on Demand), as well as image and voice broadcasting services through HFC (Hybrid Fiber Cable) transmission network. It has the structure that enables various kinds of convergence services in combination with cable internet and internet telephone.

Since the number of households subscribing to cable broadcasting services has grown to 12 million (including the digital cable broadcasting subscribers are up to 3.2 million and super-high speed internet subscribers are up to 2.8 million at present), it has played an important role of central medium for broadcasting and communication convergence service. CableLabs® which is a nonprofit research and development institute in the United States was applied in the area of technology and standards applied in the area of domestic cable. Since CableLabs® has a close technology development system with the cable broadcasting carrier, standardization and commercialization of CableLabs® have been carried out at the same time [1].

With regard to standardization of CableLabs®, economic cable data transmission which can transmit over 100 Mbps at HFC network (DOCSIS 3.0 and Modular CMTS), DOCSIS based data transmission with quality assurance (PCMM), application of downloadable contents protection system to set-top box (D-CAS, Downloadable Conditional Access System), data broadcasting for expansion of additional service, VoD expression and ads system suitable for digital broadcasting system are in progress.

In this paper, we analyzed the upstream modulation cable transmission system such as CM (Cable Modem)-to-CMTS (Cable Modem Termination System) in DOCSIS 3.0 standard and designed a RS encoder that provides variable code rates for implementing upstream modulation Gbps cable transmission system.

The remainder of this paper is organized as follows. Section 2 presents the standards of DOCSIS 3.0. In Sect. 3, we describe overall system architecture of upstream modulation Giga-level cable transmission system and slot calculation algorithm. Section 4 describes the structure of our proposed variable-rate RS encoder and burst packet generation process in different codeword modes, respectively. In Sect. 5, we report some of the simulation results. Finally, Sect. 6 concludes this paper and discusses our future direction.

2 DOCSIS 3.0 (data-over-cable interface spec. 3.0) standard

Since DOCSIS, the data transmission protocol in HFC network, has the structure of controlling each modem based on time slot using TDM (Time Division Multiplexing) for downstream and TDMA (Time Division Multiple Access) for upstream, QoS

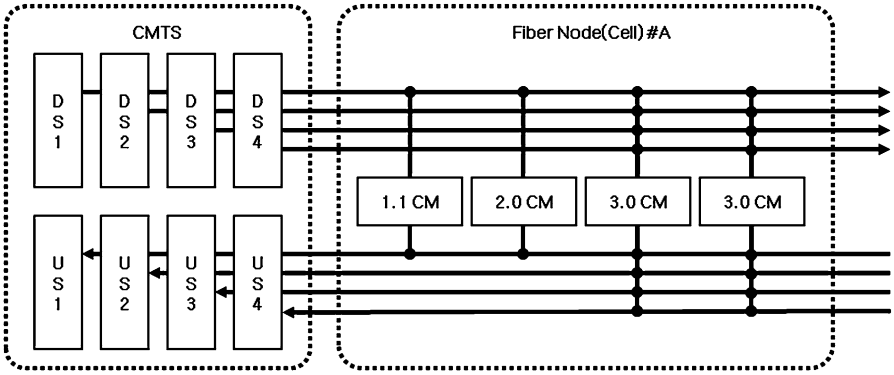


Fig. 1 The diagram of channel bonding

(Quality of Services) should be considered for multimedia data which can be very sensitive to delay or VoIP in DOCSIS Layer. Accordingly, DOCSIS has considerable advantages while data transmission based on Ethernet MAC (Media Access Control) without use of time slot is very vulnerable to QoS [4–7].

While the HFC network based internet service has been recognized as a low-speed service rather than a competing service based on Ethernet MAC due to its limit in bandwidth, it has recently prepared the opportunity to overcome the limitation with the commercialization of CMTS (Cable Modem Termination System) applied with channel bonding technology of DOCSIS 3.0 [4, 7, 8].

DOCSIS 3.0 standard, first defined in August 2006, and revised in February 2007, defines elements important for All-IP convergence based on wideband in cable network. While existing DOCSIS 2.0 supported downstream maximum 42 Mbps and upstream maximum 30 Mbps grade service using a single channel for upstream and downstream, respectively, DOCSIS 3.0 uses a technology called channel bonding, which can bond at least 4 upstream and downstream channels to combine with each channels in modem for enabling bandwidth expansion (Fig. 1). In addition, with expansion of bonding channel numbers, downstream bandwidth can be expanded up to about 42 Mbps $*$ N channels, and upstream bandwidth up to 30 Mbps $*$ N channels. For this, it defines data transmission and recombination methods for each bonding channel as main contents [4, 6, 9–11].

3 Upstream modulation Gbps cable transmission system

3.1 Upstream modulation Gbps cable transmission system

Figure 2 shows the overall concept of the Gbps cable transmission system. Upstream modulation, which transmits from CM terminal to CMTS system, uses multiple channels to transmit Giga-level data from CMTS. Data transmission is burst size transmission type and the burst size of data can be variably adjusted within the maximum size of 4,096 byte depending on the amount of data. In this paper, we design a RS encoder with variable code rate that depends on the channel status for effective protection of

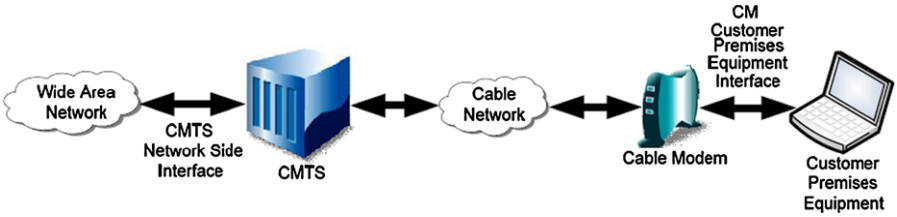


Fig. 2 The diagram of Gbps cable transmission system [4]

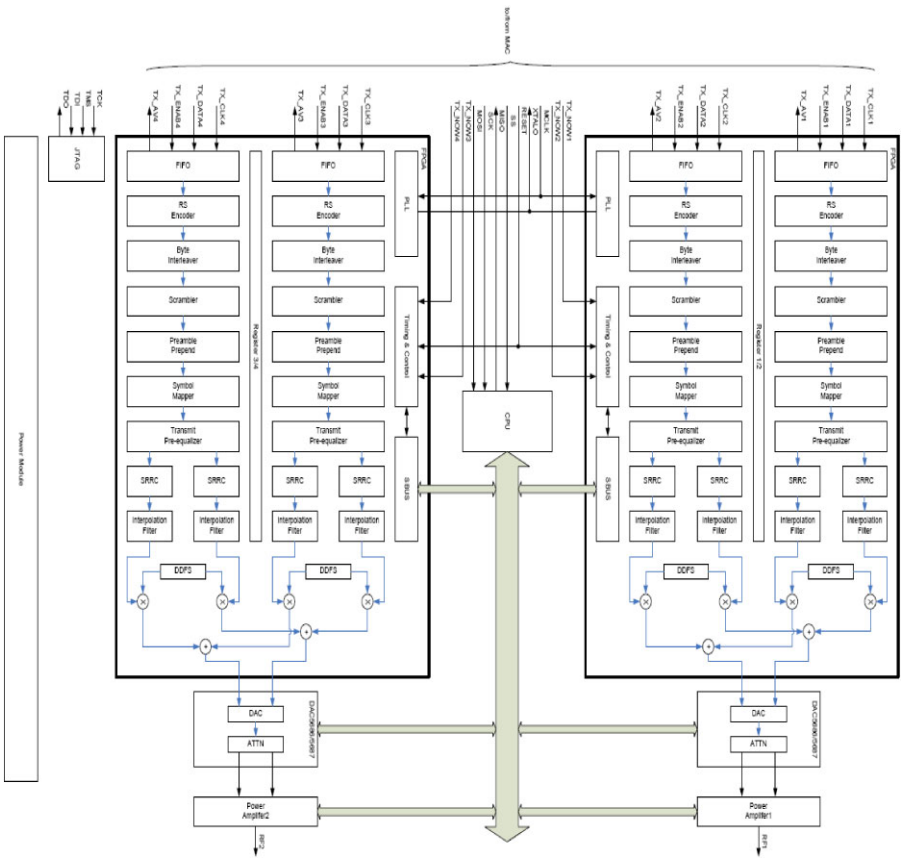


Fig. 3 The structure of upstream modulation cable transmission system

data from burst noise generated from the cable and channel coding depending on the burst size of transmission data after the modeling of a cable transmission system that uses 4 upstream modulation channels.

Figure 3 shows 4-channel cable transmission system for Giga-level transmission. The upstream modulation system consists of 2 FPGA (Field Programmable Gate Array) chips, 4 IF (Intermediate Frequency) modulators, 4 BPFs (Band Pass Filters), and 4 power amplifiers to implement 4 upstream channels. In one FPGA chip, 2 FEC

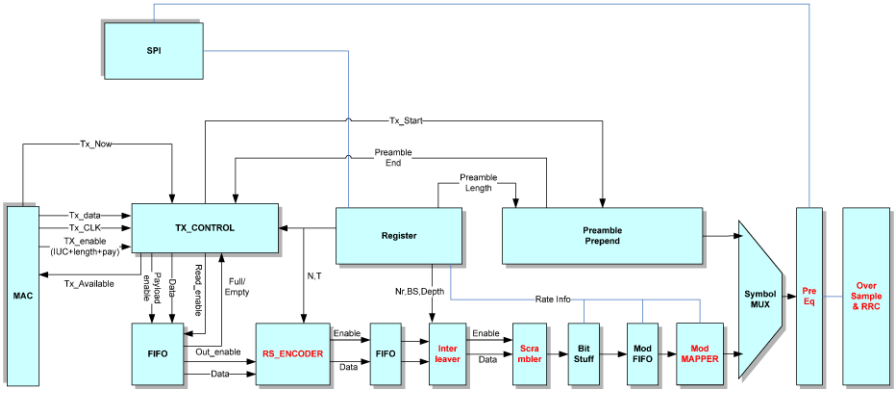


Fig. 4 The logic block diagram of single-channel upstream modulation CM system

(Forward Error Correction) encoders and 2 modulators are implemented and the IF modulator and power amplifier are designed with commercial chips or modules. Figure 4 illustrates logic block diagram of single-channel upstream modulation CM system.

Upstream modulation system is designed to have the MAC and SPI (Serial Peripheral Interface) type interfaces, independent clock from MAC for board, and the function tests, as well as to support JTAG (Joint Test Action Group) interface. In this paper, we implemented RS encoder that can take variable code rate depending on the characteristics of cable channel, in order to overcome the burst errors due to its variation of burst size transmission data in upstream cable transmission system. We also verified the function operations through simulation analysis using ModelSim and Matlab tools.

3.2 Data stuffing

When sending data through DOCSIS upstream channel, the amount of data from a terminal platform is informed by using head-end, then head-end assigns upstream channels in a way of informing proper mini-slot numbers to a terminal platform. Due to the problems listed above, the modulation sends the burst packet type data and one burst packet consists of several mini-slots. In short, burst packet is formed using time-slot called mini-slot as the basic unit. The burst packet and the power gap between the burst packets need to be reduced to transmit data in a quasi-continuous way considering effectiveness of the demodulation of head-end PHY (Physical Layer). Therefore, the data stuffing is needed during the RS (Reed–Solomon) encoding and QAM (Quadrature Amplitude Modulation) modulation process of creating a burst packet in order to match the number of assigned mini-slots as far as possible because the assigned number of mini-slots does not exactly match to the amount of data to send.

3.2.1 Byte stuffing

When the number of data assigned mini-slot will send in the RS encoding process is exceeded and RS codeword of dummy can be added to extra spare area, RS encoding is additionally conducted by doing zero/one fill. As zero/one fill is based on byte, so it is called byte stuffing.

3.2.2 Bit stuffing

FEC encoding unit (byte) and QAM modulation unit (QAM symbol) are different when modulating QAM after the process of FEC (Forward Error Correction) encoding, so zero/one fill is required enough to fill the insufficient bit in the last symbol when creating QAM symbol. At this time, zero/one fill is made by bit so it called bit stuffing. As QPSK (Quadrature Phase Shift Keying) and 16-QAM are composed of 2 bits and 4 bits by each symbol, they are multiple of FEC encoding unit (1 byte = 8 bits) so bit stuffing doesn't occur while bit stuffing occurs in case of 64-QAM.

3.3 Mini-slot calculation

A mini-slot is composed of time-tick with unconditional time gap of 6.25 μsec as the standard unit of burst duration when sending upstream burst. As mentioned in Table 1, a mini-slot capacity is variable according to M value and the symbol rate deciding the resolution of MAC's time stamp. In addition, Table 2 indicates that when the number of QAM symbols is calculated by per time-tick, QAM symbol can be obtained by mini-slot according to M value and the symbol rate [4, 12, 13].

The algorithm for calculating both the number of symbols and the mini-slots for bandwidth allocation in head-end upstream scheduler is described in detail below.

3.4 Burst packet structure

As shown in Fig. 5, the following parameters are needed to calculate the number of mini-slots for bandwidth allocation in upstream scheduler and to create the burst packet in a terminal platform:

Table 1 The mini-slot capacity

	M	Time-ticks	Mini-slot size (μsec)	QAM symbol (1280/2560/5120 ksps)
DOCSIS 2.0/3.0 (Type 5 burst descriptor)	0	1	6.25	8/16/32
	1	2	12.5	16/32/64
	2	4	25	32/64/128
	3	8	50	64/128/256
	4	16	100	128/256/512
	5	32	200	256/512/1024
	6	64	400	512/1024/2048
	7	128	800	1024/2048/4096

Table 2 The QAM symbol per time-tick

	Modulation rate (ksps)	Number of symbols
DOCSIS 3.0	1280	8
	2560	16
	5120	32

*Number of symbols = 6.25 (μsec) ∗ Modulation Rate (ksps)

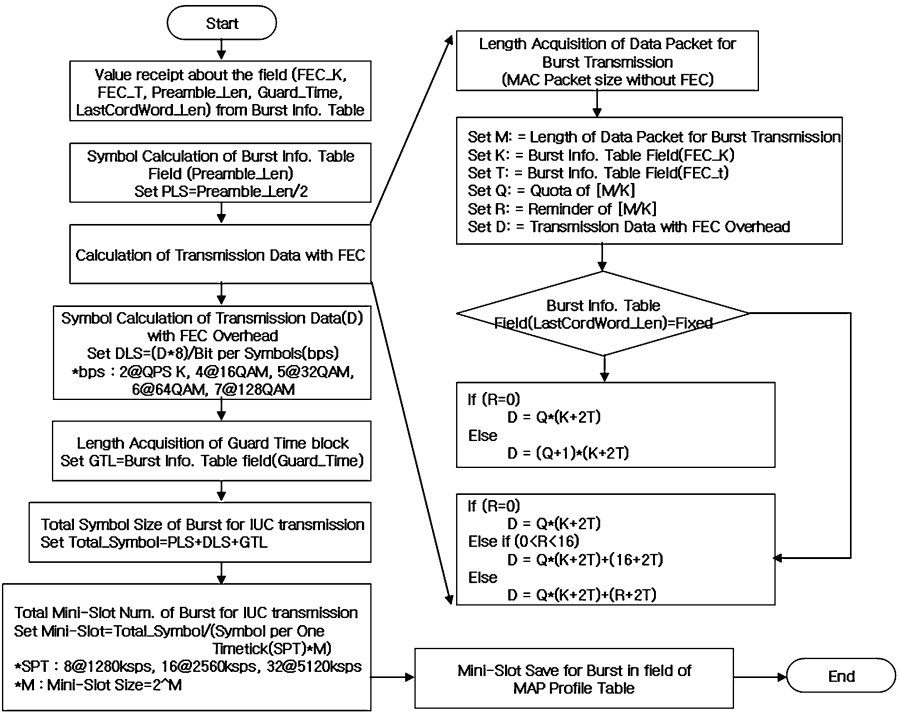


Fig. 5 The calculation algorithm of mini-slots for bandwidth allocation in upstream scheduler

- Data packet in a terminal platform will send its length
- RS encoding-related parameter (n, k, T, fixed-length codeword mode/shortened-last codeword mode)
- QAM modulation-related parameter (QAM order, symbol rate)
- Length of preamble and block length of guard time
- M value, mini-slot capacity, and the number of allocated mini-slots

To understand upstream packet creation method, firstly, it needs to look into how burst packet is constructed, using byte stuffing pattern by RS encoding and bit stuffing pattern by QAM modulation as well as ultimately the data stuffing. Figure 6 shows the burst packet structure in shortened-last codeword mode.

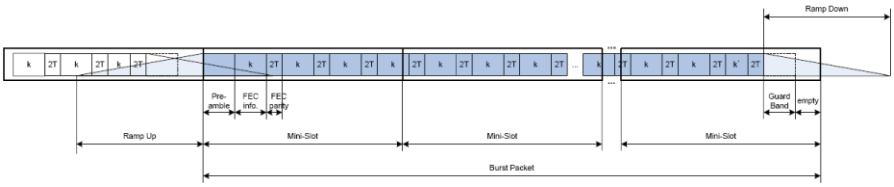


Fig. 6 The structure of burst packet data

Furthermore, this structure has shown the mini-slot capacity that is larger than RS codeword's, but the mini-slot capacity may be smaller by selecting M and n differently. Also, an empty block may not occur.

4 Variable-rate RS encoder design

As shown in Fig. 5, the number of mini-slot can be calculated as Mini-Slot = Total_Symbol/(Symbol per One Timetick (SPT) $\times$ M) and if the result value is a prime number, then the actually allocated mini-slot number will be bigger than the result value or it will take the minimum integer. The time gap may occur due to the difference between the actually allocated mini-slot number and integer; therefore, various types of byte stuffing are performed according to both each codeword mode and R value of RS encoder.

4.1 RS encoder design

The RS code is GF(q)-phased block in series with q elements. In this paper, we designed RS code as the shortened code in case of where $q = 2^8$. First, it is required to identify the characteristics of RS (n, k).

For example, RS (16, 12) is the shortened code of RS (255, 251) and RS (65, 57) is the shortened code of RS (255, 247) code. The length of data differs but the circuit is same for implementation since codeword should be created for remaining data only while first 239 and 190 data entered are regarded "0/".

Encoder functions to output n codewords with addition of $2t$ parity to k data entered for protection of data [14–16]. The encoding method is the same as the general cycle code since RS code belongs to cycle code, in general. But it differs in that the unit of data entered is not bit but 8 bits are entered as one symbol. Accordingly, the calculation of multiplier and adder is rather complicated than encoder of ordinary cycle code [17, 18].

Data entered in RS encoder for this paper corrects the error of symbol units composing of 8 bits, and all these symbols are GF(2^8) phased element. In addition, the minimum distance between the formed codewords is $n - k + 1$ and it is the maximum distance code with maximum value of singleton-bound.

- GF(2^8) with $T = 1$ to 16 or no RS encoding
- Primitive polynomial:

$$p(x) = x^8 + x^4 + x^3 + x^2 + 1$$

- Generator polynomial:

$$g(x) = (x + 2^0)(x + 2^1) \cdots (x + 2^{2T-1})$$

- RS Encoding mode
  - n: 18 to 255 bytes
  - k: 16 to 253 bytes
  - T: 1 to 16
- No RS Encoding mode
  - n: 1 to 255 bytes
  - k: 1 to 255 bytes
  - T: 0 byte

The variable-rate RS encoder, designed in this paper, supports both fixed-length codeword mode and shortened-last codeword mode and the number (k) of minimum information unit (byte) in both modes is 16. If the transmitting data length is smaller

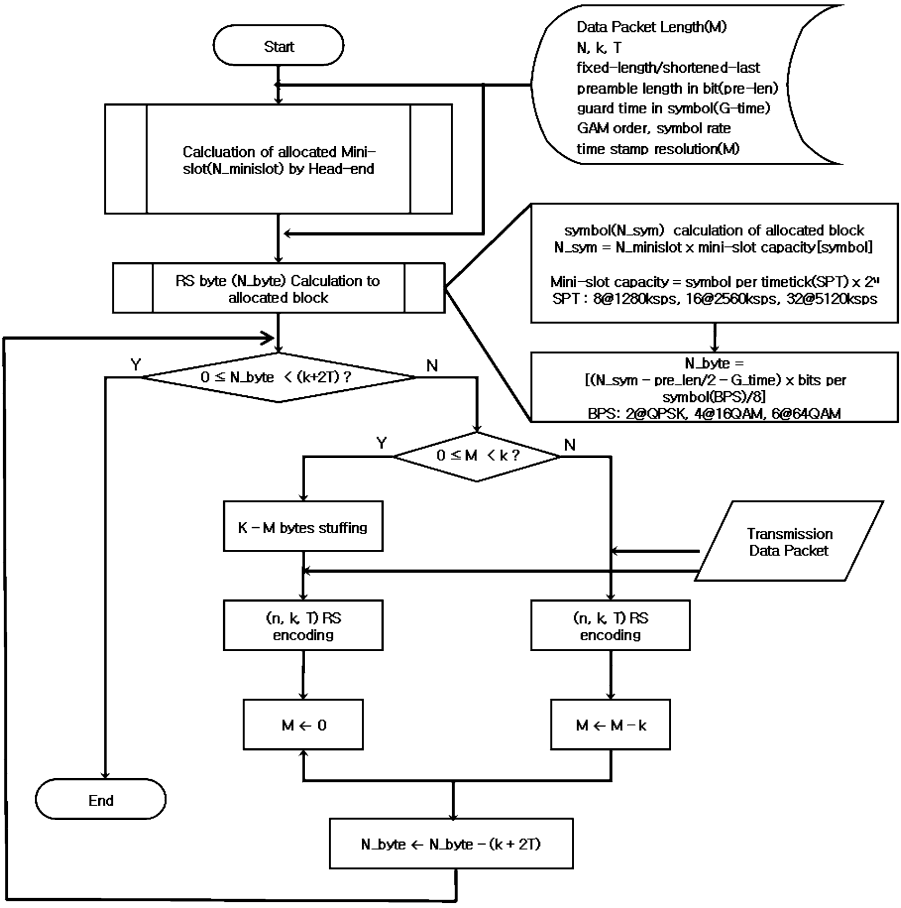


Fig. 7 The burst packet generation process in fixed-length codeword mode

than k or smaller than 16, it can be executed as follows depending on RS coding mode.

Mode 1: Fixed-length codeword mode

- In case of (Length of data to transmit $\geq k$): execute (n, k, T) RS coding
- In case of (Length of data to transmit $< k$): execute (n, k, T) RS coding after byte stuffing as much as (k—length of data to transmit)

Mode 2: Shortened-last codeword mode

- In case of (Length of data to transmit $\geq k$): execute (n, k, T) RS coding
- In case of ($16 \leq$ Length of data to transmit $< k$): execute (*Length of data to transmit* $+ 2T$, Length of data to transmit, T) RS coding
- In case of (Length of data to transmit < 16): execute $(16 + 2T, 16, T)$ RS coding after byte stuffing as much as (16—*Length of data to transmit*)

Figures 7 and 8 show the creation process of data packet in the fixed mode and the shortened mode which both are considered in this paper.

Figure 9 shows the design structure of RS encoder that supports variable code rate. As shown in Fig. 9, its structure was designed to enable the variation of codeword

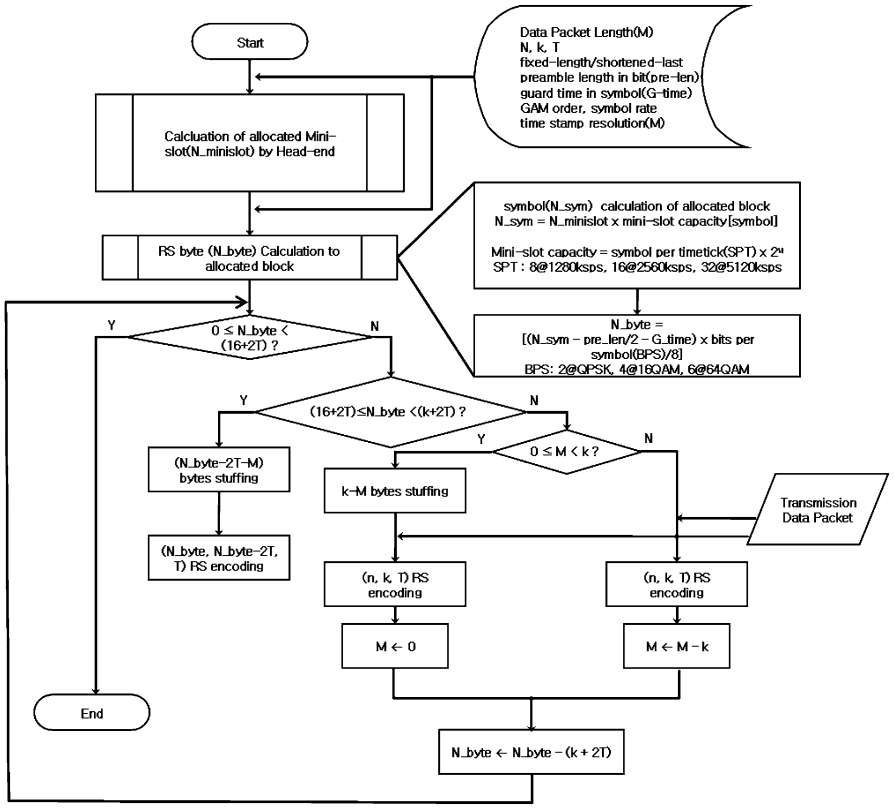


Fig. 8 The burst packet generation process in shortened-last codeword mode

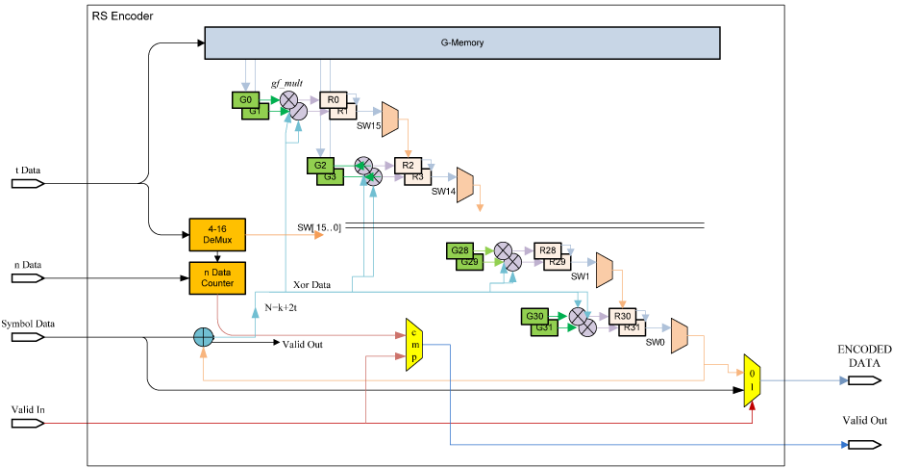


Fig. 9 The structure of variable-rate RS encoder

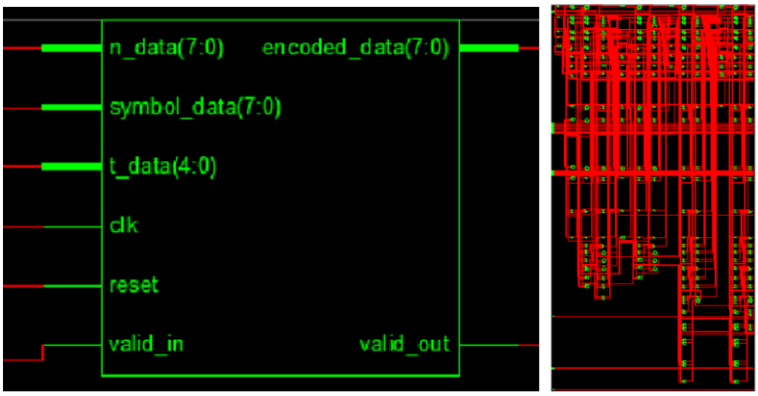


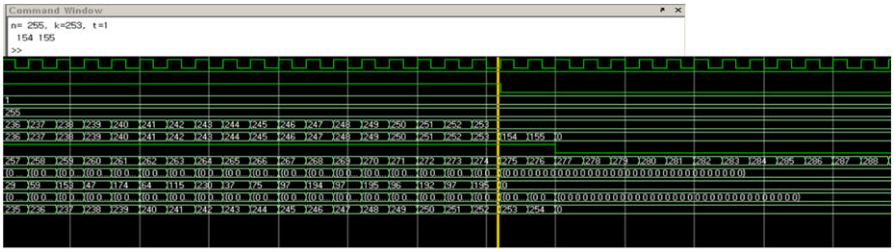
Fig. 10 The schematic block and structure of RS encoder

length n (under 255 bytes), and the variation error setting with the correction number t value between $2 \sim 16$.

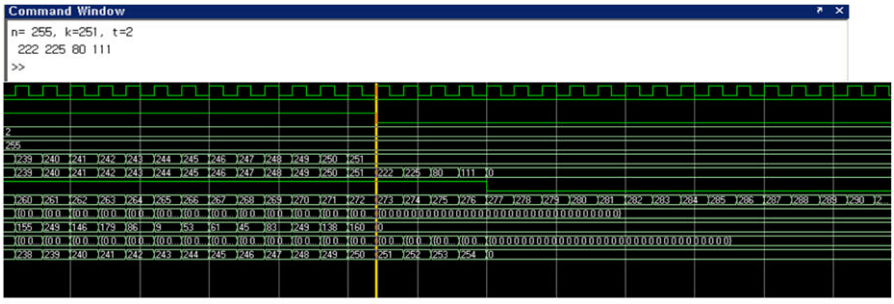
That is, it shows the RS encoder structure that can flexibly operate with variable t value. To improve the complexity of structure, it is designed to calculate and save the coefficient coming from GF(2^8) in G-memory and to execute input data and GF Mult according to this. It performs the switching operation by t value and outputs the coded parity data after passing shift register.

5 Analysis and review of simulation

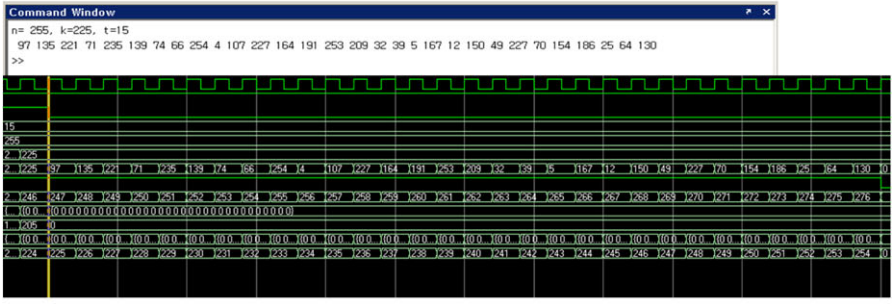
Figure 10 shows the schematic structure of the RS encoder implemented through VHDL coding using Xilinx ISE Tool.



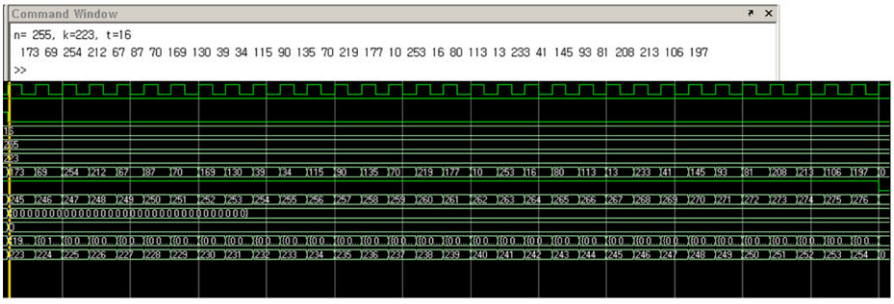
(a) RS(255,253,1) encoding process



(b) RS(255,251,2) encoding process

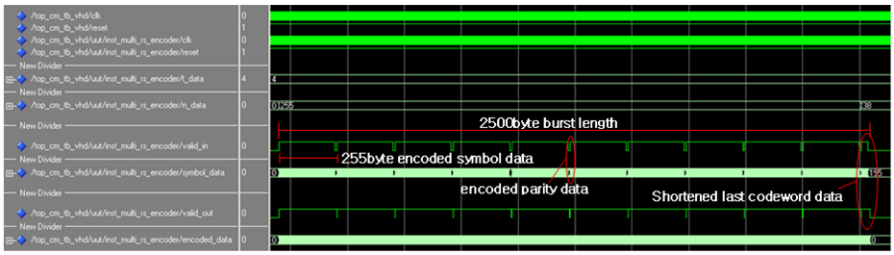


(c) RS(255,225,15) encoding process

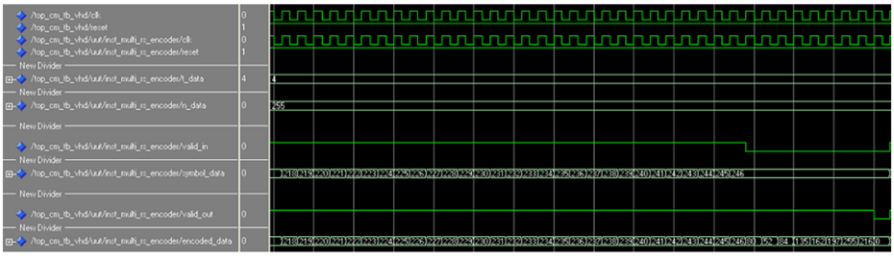


(d) RS(255,223,16) encoding process

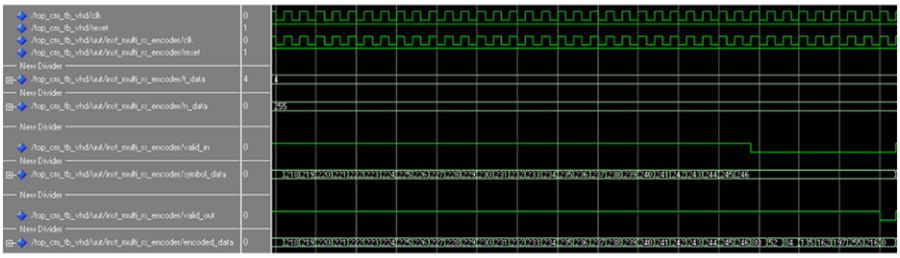
Fig. 11 The timing simulation results of RS (255, $*$) encoding according to t value



(a) Output data of RS encoder on 2500byte burst size



(b) Fixed codeword length mode ([fixed 247byte + parity(2t = 8)] * 10symbol)



(c) Shortened last codeword mode (shortened 30byte + parity(2t = 8))

(d) Output data of RS encoder (Matlab simulation)

Fig. 12 The simulation verification of variable-rate RS encoder using ModelSim and Matlab

Figure 11 shows the timing simulation results of RS encoder that supports variable coding rate. It can be identified that the result value from changing t value in RS encoder implemented with VDHL design is same as the value of parity data from RS encoder in the Matlab simulation.

Figure 12 is the example of simulation verification and shows the case when burst transmission data = 2500 bytes, $t = 4$, and $n = 255$. Since $k = 247$ at this time, coding is performed on data entered in the RS encoder in the unit of 247 bytes symbol. Accordingly, the output RS symbol is 10 symbols in 255 bytes and 1 symbol in 38 bytes, respectively. For the last symbol data in 38 bytes, encoding is performed with RS shortened code whose code rates are given as $n = 38$, $k = 30$, and $t = 4$ after entering 30 bytes of symbol data.

6 Conclusion

In this paper, we analyzed the upstream modulation cable transmission system as CM (Cable Modem)-to-CMTS in DOCSIS 3.0 standard. This study designed channel coding according to variables of burst size transmission data for the development of modulation Gigabit transmission system. In addition, it implemented RS encoder able to have the code rate as the variable according to characteristics of channels. The simulation results for verifying the function operation are obtained by means of ModelSim Tool.

While variable-rate RS encoder designed in this paper might have the shortcoming of having memory compared to existing RS encoder, its complexity of implementation was effectively improved. Moreover, it can provide the adaptive code rate depending on the characteristics of irregular channels. The burst noise error can cause high data loss, so we will design an interleaver which can perform the dynamic interleaving operation to minimize data loss in the near future.

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