Measurement of 40 power system harmonics in real-time on an economical ARM® Cortex™-M3 platform

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Within future homes and electrical power networks, emphasis is being placed on intelligent, distributed measurement devices. In particular, the recognition of individual or aggregated loads through harmonic signature has been proposed as a useful way to enhance the value of home energy monitoring/control. Clearly, the cost of implementing such measurement devices is a major barrier to acceptance. In a recent project, a challenge was set to implement real-time software on an ARM® Cortex™ LPC1768 microcontroller platform (chip cost c. £4). The software must be capable of measuring a single-phase AC frequency, real and reactive power flows and provide a full breakdown of the voltage and current (and power) behaviour via harmonic analysis from DC to the 40th, in real-time with a new output every 20 ms. In addition, the algorithm must be capable of adapting the measurement when the frequency is not nominal (50 Hz) so that spectral leakage is minimised. It is found that the LPC1768 processor is capable of supporting such an algorithm when it is coded appropriately. This knowledge de-risks the proposed use of such cheap microcontrollers for these relatively complex tasks.

Introduction: Implementation of non-invasive load monitoring (NILM) techniques within domestic and low-voltage power networks requires low-cost sensors and computational platforms. Many methods and algorithms have been proposed to enable detection and identification of loads. These tend to involve measurement of the dynamic real and reactive power flow changes during turn-on and turn-off transients [1], or harmonic signature analysis or a combination of several such techniques [2–4]. All these techniques require dynamic measurement of the current and voltage (and hence power) waveforms in real-time, including Fourier analysis or wavelet-type techniques. These are traditionally regarded as tasks of significant computational intensity, particularly when additional complications such as off-nominal frequency operation (and its effect on measurement accuracy) are considered. For example, 'recommended' implementations of phasor measurement units at transmission-level voltages still do not expect the measurement techniques to include algorithms which adapt to off-nominal frequency to minimise errors [5]. At the same time, commercial power quality meters generally contain customised hardware which can adapt the sample rate to match the system frequency, but provide very slow update rates. Both these above examples have costs in the region of high hundreds or several thousand pounds.

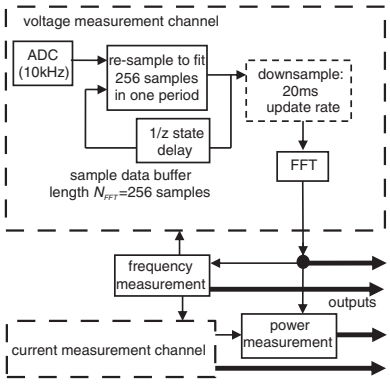

Fig. 1 *Block diagram for implemented algorithm to measure single-phase AC device (voltage and current)*

In contrast, for the NILM techniques, a sensor and processor with a cost in the low tens of pounds is probably required. To see if this can be achieved, the authors took a measurement code for a resampled fast Fourier transform (FFT), augmented it to provide frequency measurement and power measurement functions and implemented it on an ARM® Cortex™ LPC1768 microcontroller. Practically, the mbed [6] development kit was used, which integrates the central processing unit (CPU) in an easy-to-use package with interfaces etc., for around £30–40. The same CPU is also available in an LPCXpresso kit, which is slightly cheaper. The wholesale cost of the CPU in bulk is less than £4.

Algorithm method: The algorithm used is based on that proposed in [7], which was compared with discrete Fourier analysis methods in [8]. An overview is shown in Fig. 1. The most important feature to note is that this algorithm includes two stages. The first stage executes at the analogue-to-digital converter (ADC) sample rate, which is 10 kHz and above the Nyquist frequency for the 40th harmonic of 50 Hz. At the nominal 50 Hz frequency, therefore, there are 200 samples per cycle. Voltage and current samples at this rate are re-sampled using third-order interpolation, in such a manner that the re-sampled dataset places exactly 256 samples across one fundamental cycle period. Note that this period changes as the (measured) system frequency is determined.

The re-sampled datasets consist of 256 32 bit values each (1 kB for voltage and 1 kB for current), which are held in rolling memory buffers and the re-sampling algorithms use pointer arithmetic so that the new samples overwrite the oldest samples, and no 'memory copy' or 'memory shift' operations are required. The pointer to the most recent sample must be carefully tracked. This is important because after the FFT, the time-shift theorem needs to be applied in order to account for the phases of the harmonic components.

The FFT operation is triggered once every 20 ms, i.e. only once for every 200 samples sampled at the ADCs. The FFT and post-analysis code are generated using auto-generated C code from the MATLAB SIMULINK code. In particular, the standard SIMULINK FFT is used, which recognises that only real values (not complex) are input and allows the 'half length' algorithm to be used. This algorithm requires an additional memory space of 256 32 bit values in which to place the calculated real and imaginary output components, a total of 2 kB for voltage and 2 kB for current. The FFT operation is computationally intensive, and is executed at a low interrupt priority, which allows the re-sampling algorithm to be executed at 10 kHz on a higher-priority interrupt.

In this implementation, a new FFT operation is triggered exactly every 20 ms, since the main requirements were a regular measurement of frequency, harmonic content, active and reactive powers. However, an interesting point is that since the single-cycle FFT measurement has a rectangular window function, a more accurate cumulative energy monitor could be created by triggering a new FFT at a rate given by the period of the actual system frequency which varies in time. This would avoid double-counting or mis-counting of energy due to off-nominal frequency.

The main algorithm augmentations compared with the description in [8] is that a closed-loop frequency measurement was added to the voltage measurement. This is done by extracting the rate-of-change of the phase of the fundamental voltage from the FFT, and averaging over five FFT measurements (100 ms) using a simple equally weighted 5-tap FIR filter. The averaging reduces ripple due to inter-harmonics and noise, and reduces the risk of the frequency measurement loop oscillating.

Additional functions which are executed at the 20 ms rate are the calculations of the magnitude and the phase of each harmonic, RMS values, total harmonic distortion, power factors/angles and the total active power flow, which is calculated by summing all the power flows on each individual harmonic. This last part allows the calibration of sensors with known responses across the frequency range, giving a more accurate result than a simple averaged product of the instantaneous voltages and currents.

Computational viability on ARM Cortex M3: The CPU itself has a maximum clock speed of 96 MHz. The mbed platform includes 32 kB data memory (random access memory (RAM)) and 512 kB Flash memory, although the CPU itself can support up to 64 kB RAM [6]. Power consumption is of the order of 7–149 μW/MHz [9]. The key question is whether the described algorithm can be executed on the microcontroller within the 20 ms allowed for the analysis of each single cycle. Initial benchmarking results suggested that the ARM CPU was slower than the more expensive Infineon TC1796 processor [8] by a factor of between 3 (multiplication and division) and 10 (trigonometric functions). However, by adopting all the optimisations described in this Letter and in [8], it is found possible to execute the resampling algorithm (for both voltage and current channels) in about

54 μs, within the maximum allowed time of 100 μs to support 10 kHz sampling.

The time required to execute the two channels of FFT is much longer. First, the FFT requires more mathematics as is well known. In addition, the two FFTs access the full 6 kB of memory, which itself takes time. The two FFTs take 8720 μs in total. This is within the 20 000 μs (20 ms) limit. Crucially, the total of $200 \times 54\ \mu s + 8720\ \mu s = 19\ 520\ \mu s$ is marginally within the total allowed limit of 20 ms allowed to make the entire operation viable with the sampling and re-sampling at 10 kHz.

Conclusion: We find that it is possible (by a tight margin) to sample a single-phase AC waveform (both voltage and current) at 10 kHz and perform a thorough analysis of its properties on a cycle-by-cycle basis, on a modern but cheap microcontroller such as the ARM® Cortex™-M3, with a low power consumption. The analysis includes Fourier analysis to the 40th harmonic, with minimal spectral leakage due to the re-sampling process. Knowledge of this possibility allows the creation of economical but highly accurate and capable distributed sensors within domestic environments.

24 January 2013
doi: 10.1049/el.2013.0299
One or more of the Figures in this Letter are available in colour online.

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