Dual operation characteristics of resistance random access memory in indium-gallium-zinc-oxide thin film transistors

Jyun-Bao Yang,[1] Ting-Chang Chang,[1,2,3,a)] Jheng-Jie Huang,[2] Yu-Chun Chen,[2] Yu-Ting Chen,[1] Hsueh-Chih Tseng,[2] Ann-Kuo Chu,[1] and Simon M. Sze[2,4]
[1]*Department of Photonics, National Sun Yat-Sen University, Kaohsiung, Taiwan*
[2]*Department of Physics, National Sun Yat-Sen University, Kaohsiung, Taiwan*
[3]*Advanced Optoelectronics Technology Center, National Cheng Kung University, Taiwan*
[4]*Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan*

(Received 25 February 2014; accepted 30 March 2014; published online 14 April 2014)

In this study, indium-gallium-zinc-oxide thin film transistors can be operated either as transistors or resistance random access memory devices. Before the forming process, current-voltage curve transfer characteristics are observed, and resistance switching characteristics are measured after a forming process. These resistance switching characteristics exhibit two behaviors, and are dominated by different mechanisms. The mode 1 resistance switching behavior is due to oxygen vacancies, while mode 2 is dominated by the formation of an oxygen-rich layer. Furthermore, an easy approach is proposed to reduce power consumption when using these resistance random access memory devices with the amorphous indium-gallium-zinc-oxide thin film transistor. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4871368]

Amorphous metal oxide-based semiconductors (AOSs) have demonstrated the benefits of applications as thin film transistors (TFTs) in next generation displays due to their superior electrical performance, visible light transparency, and tunable carrier concentrations even when deposited at room temperature.[1–3] During the past few years, amorphous indium-gallium-zinc-oxide (a-IGZO) has been intensively studied for adoption as the channel material in TFTs to replace amorphous silicon, especially for large area display applications. The a-IGZO TFTs exhibit high field-effect mobility and low off-state current, which meet the high frame rate and lower power consumption requirements for displays.[4–8] In particular, because of their high electron mobility and uniformity, all multifunctional devices can be integrated on a display panel, as known as system-on-panel (SOP). In addition, though memory devices are essential to SOP, they require a more complex process and hence more expensive fabrication.[9] Hence, a-IGZO TFTs, which can simultaneously exhibit transistor and Resistance random access memory (RRAM) characteristics, are of crucial importance. RRAM is one of the most promising candidates to be adopted in next-generation nonvolatile memory,[10–16] and has many advantages such as low power consumption, fast switching speed, and high density.[17–22] From previous research,[23,24] IGZO was found to have resistance switching (RS) characteristics.

In this study, staggered bottom gate via-type a-IGZO TFTs are fabricated on glass substrate. First, after a 150-nm-thick Mo film deposition as gate electrodes by sputtering, a 300-nm-thick SiO_x film is deposited as gate insulator (GI) using plasma enhanced chemical vapor deposition (PECVD). Then a 50-nm-thick a-IGZO film was deposited as the channel layers by sputtering at room temperature, using a target of In_2O_3:Ga_2O_3:ZnO = 1:1:1 in atomic ratio. A 200-nm-thick SiO_x etching stop layer was deposited by PECVD. The source (S) /drain (D) electrodes were formed by sputtering 150-nm-thick Mo. A 100-nm-thick SiO_x and SiN_x film were sequentially deposited as the passivation layer using PECVD. The device dimensions are channel width/length of 10 μm/10 μm. Finally, the devices were annealed in an oven in atmospheric ambient and the device was completed as shown in Fig. 1(c). All electrical measurements were performed in the dark at room temperature using an Agilent B1500 semiconductor parameter analyzer and a Cascade M150 probe station. The threshold voltage (V_T) was determined by the constant current method as the gate voltage (V_G) which induces drain current (I_D) of 1 nA, and subthreshold swing (S.S.) was determined by the equation $S.S. = dV_{GS}/d\ (\log I_D)$ (V/decade) in the current range of 10^{-11} to 10^{-9} A.

Figure 1(a) shows the I_D-V_G transfer electrical characteristic of a-IGZO TFTs with drain voltages (V_D) of 0.5 V and 10 V. The device exhibits good electrical characteristics with $V_T = 0.2$ V, S.S. = 0.14 V/decade, and mobility of 11.6 $cm^2/V{\cdot}s$. Figure 1(b) shows I_D-V_D characteristics with V_G of 2, 4, 6, 8, and 10 V. It indicates that the I_D-V_D characteristics show good Ohmic behavior without current crowding at low drain voltages, and the contact resistance between S/D electrodes and a-IGZO is low enough to be negligible.

As for RRAM characteristics, in order to form the conduction paths in the RS layer (a-IGZO) and demonstrate the RS property, the a-IGZO film must undergo a soft-breakdown (forming) process.[25] According to the structure of the a-IGZO TFT and current paths, the equivalent circuit in a TFT device can be considered as three resistors (R_S, R_C, and R_D) in series, as shown in Fig. 2(a). The R_C is the resistor of channel and the R_S and R_D are the resistors between source and drain to channel, respectively. Because the length between the source and drain is 10 μm, it is difficult to break down the a-IGZO film laterally with a floating gate, as shown in Fig. 2(b). However, the applied gate voltage can accumulate carriers in the channel and reduce the channel

a)tcchang@mail.phys.nsysu.edu.tw

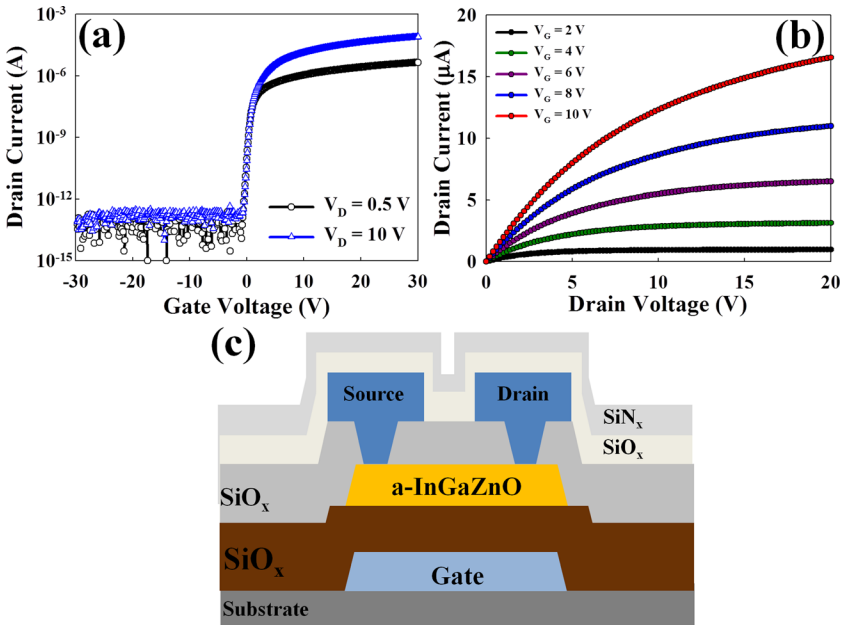

FIG. 1. (a) ID-VG transfer characteristics of the a-IGZO TFT in VD = 0.5 V and VD = 10 V. (b) ID-VD characteristics of a-IGZO TFT with VGate of 2 V, 4 V, 6 V, 8 V, and 10 V. (c) Cross-sectional view of the a-IGZO TFT device.

resistance. Hence, the applied drain voltage can induce strong vertical electric field near drain region and breakdown the a-IGZO film along the vertical direction (R_S and R_D), as shown in Fig. 2(b). Near the drain region, due to the strong vertical electric field during the forming process, oxygen ions can be formed by breaking the metal-oxide bonds and can further migrate downward and congregate at the IGZO/GI interface as shown in Fig. 2(c). Hence, the conduction path near the drain region is composed of oxygen vacancies.[26] In contrast, near the source region, oxygen ions migrate upward and congregate at the IGZO/source electrode interface. Therefore, an oxygen-rich layer is

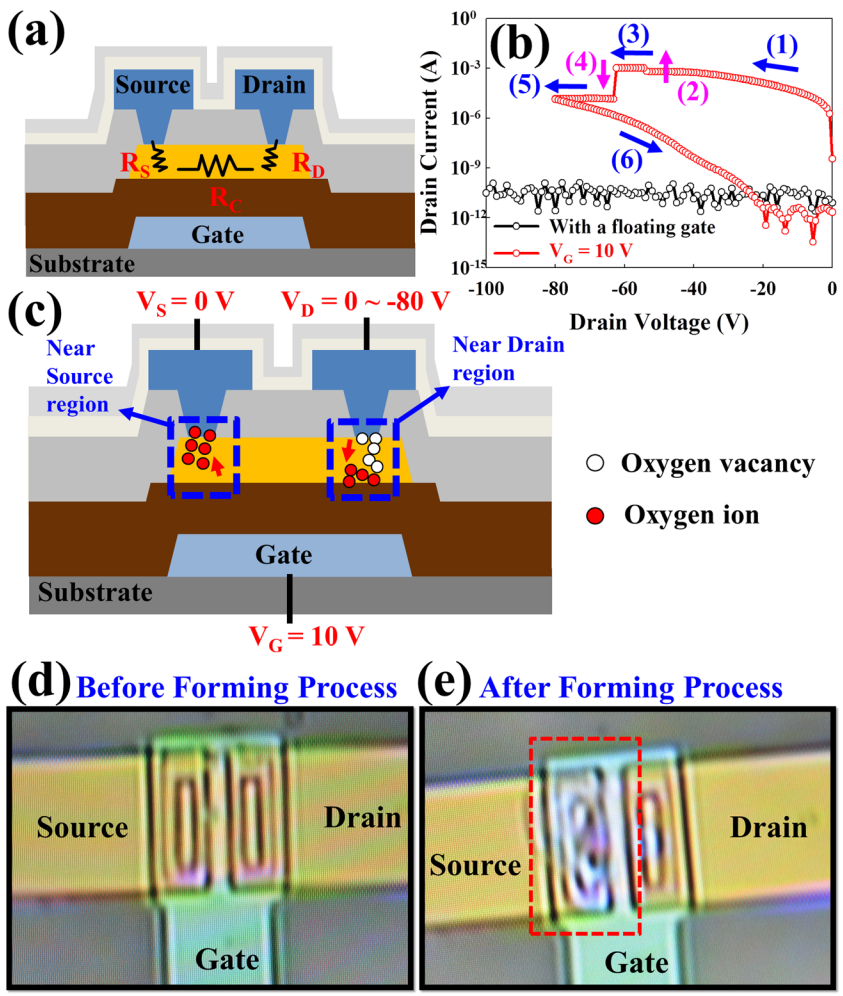

FIG. 2. (a) Structure and equivalent circuit of the a-IGZO TFT device. (b) Current-voltage characteristics during forming process with a floating gate or 10 V of gate bias (c) Illustration of oxygen ion migration during the forming process. Top view image of a-IGZO TFT (d) before and (e) after the forming process.

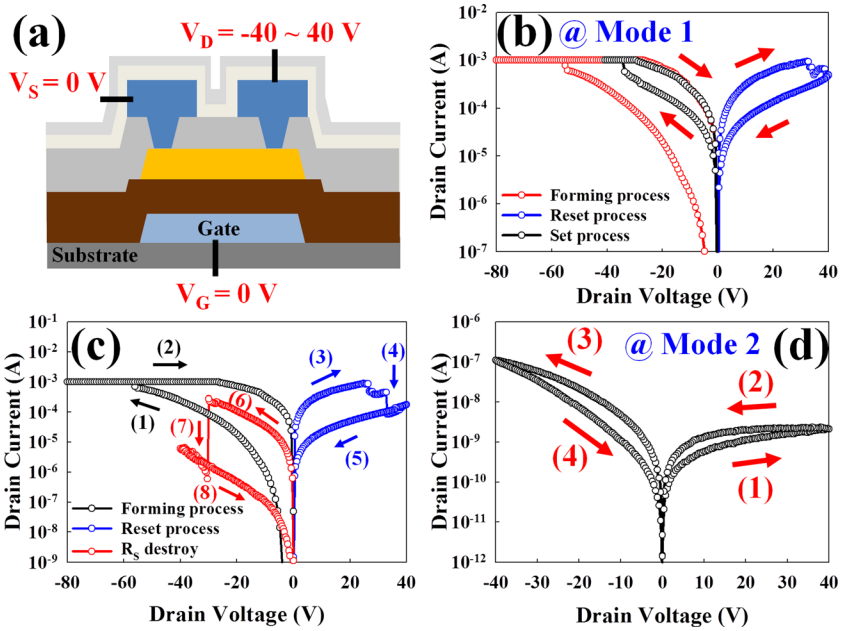

FIG. 3. (a) Illustration of the sweeping operation condition. (b) I-V curves of mode 1 resistance switching characteristics. (c) Transformation from mode 1 to mode 2. (d) I-V curves of mode 2 resistance switching characteristics.

formed at the interface of the source electrode and IGZO.[27,28] Furthermore, the contact between source electrode and a-IGZO film is separated due to this oxygen migration, as shown in Figs. 2(d) and 2(e).

From the current-voltage (I-V) curves of the forming process, it is found that the current clearly increases at step 2 and rapidly decreases at step 4, as shown in Fig. 2(b). In order to hold the resistance state at step 2 in Fig. 2(b), the DC drain voltage sweeping is carried out with 1 mA compliance current to soft-breakdown the a-IGZO film, as shown in Fig. 3(b). Subsequently, as shown in Fig. 3(a), the source and drain are grounded, and the DC sweeping of drain voltage with 1 mA of compliance current is performed to switch the resistance state. The RS behavior exhibits the bipolar switching characteristic after forming process with 1 mA of compliance current, shown in Fig. 3(b). The current decreases as the applied drain voltage is swept from 0 V to 40 V, whereas the current increases when the drain voltage is swept from 0 V to −40 V. This bipolar switching characteristic is defined as mode 1. After several switching cycles, shown in Fig. 3(c), the current rapidly decreases at step 7. The RS behavior then changes to mode 2, shown in Fig. 3(d). The resistance value of mode 2 can be switched to low resistance and high resistance states by positive and negative bias, respectively. Furthermore, it is found that the mode 2 RS behavior can also be observed if the device initially undergoes forming process without compliance current (step 4 in Fig. 2(b)).

According to the applied electric field and RS characteristics, the RS mechanism in the a-IGZO TFT-based RRAM device is proposed as in Fig. 4 to explain how the resistance value switches. During the forming process, the applied strong vertical electric field breaks the metal-oxide bonds at drain and source regions and produces oxygen ions. After the oxygen ion migration, the oxygen-rich layer is formed near the source interface and the conduction path composed of oxygen vacancies is formed near the drain region, as shown in Fig. 4(a). Mode 1 is dominated by the formation/rupture of the conduction path near the drain region. As positive bias is applied to the drain electrode, the oxygen ions migrate toward the drain and recombine with oxygen vacancies, resulting in the rupture of the conduction path (reset process). In contrast, the oxygen vacancy conduction path can be re-formed by an applied negative drain bias (set process). Accordingly, R_D increases as the conduction path

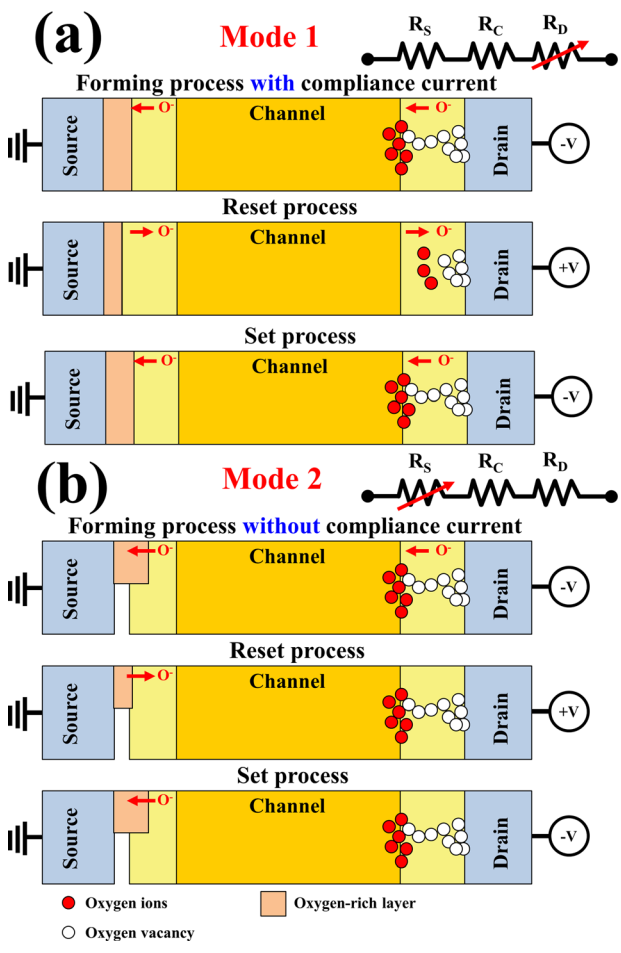

FIG. 4. Resistance switching mechanism of (a) Mode 1 and (b) Mode 2 during the forming, reset, and set processes.

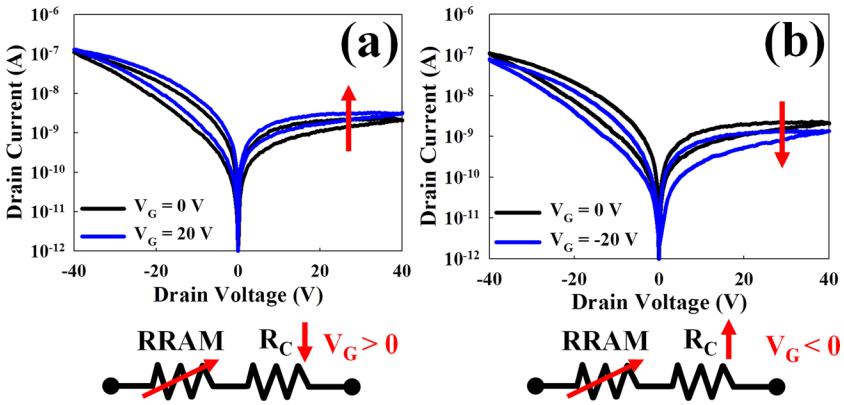

FIG. 5. Resistance switching characteristics are controlled by (a) positive and (b) negative gate biases.

ruptures and decreases as the conduction path re-forms, and these switching cycles can be repeated.

Furthermore, the resistance value of the oxygen-rich layer (R_O) is equal to $\rho \frac{L_O}{A_O}$. The ρ, L_O, and A_O are the resistivity, thickness, and area of the oxygen rich layer, respectively. Initially, the R_O is very small because of the large contact area, and therefore the RS behavior is dominated by the oxygen vacancies near the drain region. However, the accumulation of oxygen ion can damage the source electrode contact and reduce the contact area, causing an increase in the resistance value of the oxygen-rich layer. Therefore, the RS of mode 2 is mainly controlled by the thickness of the oxygen-rich layer, so R_O plays the dominant role in the RS behavior, as shown in Fig. 4(b).

In order to reduce the power consumption, it is essential to decrease the operating current. Because the channel path is a RRAM and R_C in series, the operating current in controlled by the R_C which can be modulated by gate bias. As positive bias is applied to the gate, the operating current increases because the resistance value of R_C decreases, as shown in Fig. 5(a). Hence, the operating current can also be decreased when a negative bias is applied to the gate since the resistance value of R_C is increased, as shown in Fig. 5(b).

In summary, two kinds of RS characteristics are present in the a-IGZO TFT after the forming process, both due to oxygen ion migration near the source and drain region. Mode 1 switching behavior is dominated by the formation/rupture of the conduction path composed of oxygen vacancies, while mode 2 is dominated by the thickness of the oxygen-rich layer. In addition, the operating current can be controlled by gate bias, which offers an approach to reduce power consumption.

This work was performed at National Science Council Core Facilities Laboratory for Nano-Science and Nano-Technology in Kaohsiung-Pingtung area, NSYSU Center for Nanoscience and Nanotechnology, and was supported by the National Science Council of the Republic of China under Contract No. NSC-102-2120-M-110-001.

[1]H. Hosono, J. Non-Cryst. Solids **352**, 851 (2006).
[2]E. Fortunato, P. Barquinha, A. Pimentel, A. Goncalves, A. Marques, L. Pereira, and R. Martines, Adv. Mater (Weinheim Ger) **17**, 590 (2005).
[3]P. Gorrn, M. Lehnhardt, T. Riedl, and W. Kowalsky, Appl. Phys. Lett. **91**, 193504 (2007).
[4]C. T. Tsai, T. C. Chang, S. C. Chen, L. Lo, S. W. Tsao, M. C. Hung, J. J. Chang, C. Y. Wu, and C. Y. Huang, Appl. Phys. Lett. **96**, 242105 (2010).
[5]T. C. Chen, T. C. Chang, C. T. Tsai, T. Y. Hsieh, S. C. Chen, C. S. Lin, M. C. Hung, C. H. Tu, J. J. Chang, and P. L. Chen, Appl. Phys. Lett. **97**, 112104 (2010).
[6]J. B. Kim, C. Fuentes-Hernandez, W. J. Potscavage, Jr., X. H. Zhang, and B. Kippelen, Appl. Phys. Lett. **94**, 142107 (2009).
[7]T. C. Chen, T. C. Chang, T. Y. Hsieh, W. S. Lu, F. Y. Jian, C. T. Tsai, S. Y. Huang, and C. S. Lin, Appl. Phys. Lett. **99**, 022104 (2011).
[8]D. K. Seo, S. Shin, H. H. Cho, B. H. Kong, D. M. Whang, and H. K. Cho, Acta Mater. **59**, 6743 (2011).
[9]T. C. Chang, F. Y. Jian, S. C. Chen, and Y. T. Tsai, Mater. Today **14**, 608 (2011).
[10]Y. E. Syu, T. C. Chang, T. M. Tsai, Y. C. Hung, K. C. Chang, M. J. Tsai, M. J. Kao, and S. M. Sze, IEEE Electron Device Lett. **32**, 545 (2011).
[11]H. Y. Lee, P. S. Chen, T. Y. Wu, C. C. Wang, P. J. Tzeng, C. H. Lin, F. Chen, M. J. Tsai, and C. Lien, Appl. Phys. Lett. **92**, 142911 (2008).
[12]C. Y. Lin, C. Y. Wu, C. Y. Wu, C. Hu, and T. Y. Tseng, J. Electrochem. Soc. **154**, G189 (2007).
[13]T. M. Tsai, K. C. Chang, T. C. Chang, Y. E. Syu, K. H. Liao, B. H. Tseng, and S. M. Sze, Appl. Phys. Lett. **101**, 112906 (2012).
[14]K. C. Chang, R. Zhang, T. C. Chang, T. M. Tsai, J. C. Lou, J. H. Chen, T. F. Young, M. C. Chen, Y. L. Yang, Y. C. Pan *et al.*, IEEE Electron Device Lett. **34**(5), 677–679 (2013).
[15]Y. E. Syu, T. C. Chang, T. M. Tsai, G. W. Chang, K. C. Chang, J. H. Lou, Y. H. Tai, M. J. Tsai, Y. L. Wang, and S. M. Sze, IEEE Electron Device Lett. **33**(3), 342–344 (2012).
[16]S. B. Long, C. Cagli, D. Ielmini, M. Liu, and J. Sune, J. Appl. Phys. **111**(7), 074508 (2012).
[17]Y. E. Syu, T. C. Chang, J. H. Lou, T. M. Tsai, K. C. Chang, M. J. Tsai, Y. L. Wang, M. Liu, and Simon M. Sze, Appl. Phys. Lett. **102**, 172903 (2013).
[18]K. C. Chang, T. M. Tsai, R. Zhang, T. C. Chang, K. H. Chen, J. H. Chen, T. F. Young, J. C. Lou , T. J. Chu, C. C. Shih *et al.*, Appl. Phys. Lett. **103**, 083509 (2013).
[19]K. C. Chang, T. M. Tsai, T. C. Chang, H. H. Wu, J. H. Chen, Y. E. Syu, G. W. Chang, T. J. Chu, G. R. Liu, Y. T. Su *et al.*, IEEE Electron Device Lett. **34**(3), 399–401 (2013).
[20]Y. T. Chen, T. C. Chang, J. J. Huang, H. C. Tseng, P. C. Yang, A. K. Chu, J. B. Yang, H. C. Huang, D. S. Gan, M. J. Tsai, and S. M. Sze, Appl. Phys. Lett. **102**, 043508 (2013).
[21]S. K. Kim, B. J. Choi, K. J. Yoon, Y. W. Yoo, and C. S. Hwang, Appl. Phys. Lett. **102**, 082903 (2013).
[22]F. Kurnia, C. Liu, C. U. Jung, and B. W. Lee, Appl. Phys. Lett. **102**, 152902 (2013).
[23]M. C. Chen, T. C. Chang, C. T. Tsai, S. Y. Huang, S. C. Chen, C. W. Hu, S. M. Sze, and M. J. Tsai, Appl. Phys. Lett. **96**, 262110 (2010).
[24]C. H. Hsu, Y. S. Fan, and P. T. Liu, Appl. Phys. Lett. **102**, 062905 (2013).
[25]J. J. Huang, T. C. Chang, J. B. Yang, S. C. Chen, P. C. Yang, Y. T. Chen, H. C. Tseng, S. M. Sez, A. K. Chu, and M. J. Tsai, IEEE Electron Device Lett. **33**, 1387 (2012).
[26]A. Sawa, Mater. Today **11**, 28 (2008).
[27]Y. Wang, X. Qian, K. Chen, Z. Fang, W. Li, and J. Xu, Appl. Phys. Lett. **102**, 042103 (2013).
[28]W. Banerjee, S. Maikap, C. S. Lai, Y. Y. Chen, T. C. Tien, H. Y. Lee, W. S. Chen, F. T. Chen, M. J. Kao, M. J. Tsai, and J. R. Yang, Nanoscale Res. Lett. **7**, 194 (2012).