Two-transistor and two-magnetic-tunnel-junction multi-level cell structured spin-transfer torque magnetic random access memory with optimisations on power and reliability

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A two-transistor and two-magnetic-tunnel-junction (MTJ) multi-level cell (MLC) structure of spin-transfer torque magnetic random access memory (STT-RAM) is proposed. Compared with the conventional one-transistor and two-magnetic-tunnel-junction MLC STT-RAMs, by adding an extra access transistor and adjusting the connection of the two MTJs, the extra write power consumption on the soft bit MTJ can be reduced, which will also have a benefit to the lifetime of the soft bit. Specifically, the simulation results show that more than 75% write power consumption on the soft bit can be wiped out, and the area cost caused by the extra access transistor is negligible.

Introduction: Recently, spin-transfer torque magnetic random access memory (STT-RAM) obtained increasing attentions because of its unique characteristics such as non-volatility, high integration density and operation speed. For a time, many studies have been focused on single-level cell (SLC) STT-RAM for its simple structure. However lately, driven by the desire of integrating higher density, multi-level cell (MLC) STT-RAM attracts more and more attentions.

In the conventional SLC STT-RAM, the basic memory cell contains one-transistor and one-magnetic-tunnel-junction (1T1MTJ), and data is stored as two resistance states of a magnetic-tunnel-junction (MTJ) device and the resistance can switch between the low (RL) and the high states (RH) under a critical switching current (I_c) flowed from different directions. The difference between the RL and the RH is defined by tunnelling magneto resistance (TMR) ratio as TMR = (RH−RL)/RL. Table 1 shows some basic parameters of MTJ [1], Figs. 1*a* and *b* present the details of memory cell structure and MTJ device structure [2].

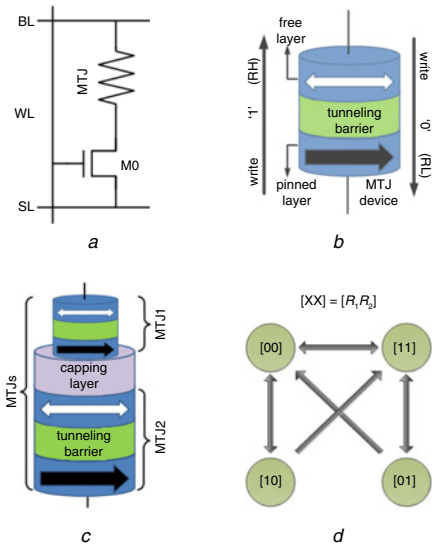

Fig. 1 *Conventional STT-RAM cell structure, MTJ device structure both in SLC and MLC and write procedure of MLC STT-RAM*

a Conventional STT-RAM cell structure
b Structure of SLC MTJ device and its operation principle
c Structure of MLC MTJ device
d Write procedure of MLC STT-RAM

Table 1: Basic parameters of MTJ device

Parameter	Description	Default value
TMR(0)	TMR ratio with 0 V_{bias}	120%
R–A	resistance–area product	5 Ω μm^2
J_c	critical current density	0.5×10^6 A/cm^2

The only difference between MLC and SLC STT-RAMs is that the MTJ device in MLC actually contains two MTJs in series, the details are presented in Fig. 1*c* [2]. As there are two different MTJs in MLC, MTJ1 (soft bit) with smaller size, relative high resistance (R_1: R_1H, R_1L) and required lower critical switching current I_{c1}; MTJ2 (hard bit) with larger S, relative low resistance (R_2: R_2H, R_2L) and required higher critical switching current I_{c2}, a two-bit data can be stored in one MLC STT-RAM cell using a two-step method [3]. The basic operate principle is described as follows.

To write data '11' into the cell, source line (SL) and bit line (BL) should be set to high voltage state (VDD) and ground (GND), respectively, as a result, a higher write current I_{wh} ($I_{wh} > I_{c2} > I_{c1}$) is generated and used to switch the two MTJs to R_1H and R_2H. Similarly, data '00' can be set into the cell by I_{wh} flowed from BL to SL. However, as the write current I_{wh} is required higher than I_{c2} ($I_{c2} > I_{c1}$), the current (I_{wh}) flowed through MTJ1 is excessive than its required (I_{c1}) obviously, which will lead to extra power consumption and lifetime degeneration on MTJ1 [4].

To write data '01' and '10' into the storage cell, a two-step write method is needed. To write data '01', the storage cell must be set to '11' firstly, then SL and BL must be set to a middle voltage state between VDD and GND (V_m) and GND, by this way, a low write current I_{ws} ($I_{c2} > I_{ws} > I_{cl}$) is produced and used to switch the soft bit MTJ1 to R_1L and the data stored in the storage cell is changed from '11' to '01'. To write data '10', the storage cell must be set to '00' firstly, then SL and L must be set to GND and V_m, by this way, a low write current I_{ws} ($I_{c2} > I_{ws} > I_{c1}$) is produced and used to switch the soft bit MTJ1 to R_1H, and the data storage in the storage cell is changed from '00' to '10'. Fig. 1*d* summarises the write procedure of MLC STT-RAM [2].

Aimed at the extra power consumption of the soft bit, a two-transistor and two-magnetic-tunnel-junction (2T2MTJ) MLC cell is proposed in this Letter. On the basis of this cell structure, the extra write power can be reduced obviously.

Proposed cell (PC): The proposed 2T2MTJ MLC STT-RAM and MLC MTJs are shown in Fig. 2, compared with conventional series MLC STT-RAM, the access transistor M0 with width $W0$ in conventional series MLC is replaced by two access transistors M1 and M2 (with widths $W1$ and $W2$), and the two different size MTJs (MTJ1 and MTJ2) exchange their location, moreover, the drain line of additional transistor M2 is connected to the MLC MTJs in the middle node. As M1 and M2 take the place of M0 and the drive current of transistor is almost directly proportional to its width, as long as we keep $W0 = W1 + W2$, the PC can drive the same two MTJs in the conventional MLC. As a result, the cost of cell area is limited [5].

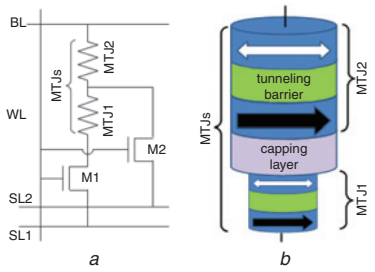

Fig. 2 *Proposed MLC cell structure and MTJ device*

a Proposed MLC cell structure
b MTJ device structure in *PC*

Before we discuss the operation principle of the PC, first some parameters must be set. To gain relatively good resistance distributions of the four resistance states, the size (S) of MTJ1 and MTJ2 are set as $S1$ and $S2$, and $S2 = 2S1$ [6], as a result, $I_{c2} = 2I_{c1}$ and $R_1 = 2R_2$ (R_1L = $2R_2$L, R_1H = $2R_2$H).

To write data '11' into the cell, SL1, SL2 and BL are connected to VDD, VDD and GND, respectively. In this process, the total write current I_{w11} ($>I_{c2}$) flowed through MTJ2 is the sum of the current $I_{w11(M1)}$ ($>I_{c1}$, flowed through M1 and MTJ1) and $I_{w11(M2)}$ (flowed through M2). As $I_{w11(M1)}$ is lower than I_{w11}, the extra write current ($I_{w11(M2)}$) flowed through MTJ1 in the conventional MLC cell is reduced. In contrast, to write data '00', SL1, SL2 and BL are connected to GND, GND and VDD, respectively. By this way, a total write current I_{w00} ($>I_{c2} > I_{c1}$) flowed through MTJ2 is generated and used to write '0' (R_2L) to MTJ2, then I_{w00} is divided into two parts, $I_{w00(M1)}$ ($>I_{c1}$) and $I_{w00(M2)}$, which flow through M1 and M2, respectively. Moreover,

MTJ1 is switched to '0' (R_1L) by $I_{w00(M1)}$, then data '00' is put into the cell.

To write data '01' and '10', the two-step write method is also needed. First, data '11' and '00' are set into the PC as mentioned above. Secondly, SL2 of M2 is separated to the circuit, so the PC is actually a conventional MLC cell, the rest operations are just the same as the conventional one.

As mentioned above, the extra power consumption caused by $I_{wxx(M2)}$ can be reduced in the whole write process, which will reduce the extra power consumption and avoid the lifetime degeneration on the soft bit.

Simulation results: To check the feasibility of the PC, a simulation is carried out using 45 nm low power COMS technology of predictive technology model. The parameters of MTJ1 and MTJ2 calculated by Table 1 and used in this simulation are shown in Table 2.

Table 2: Parameters of MTJ1 and MTJ2 used in simulation

Parameter	Size (nm^2)	RH (kΩ)/RL (kΩ)	I_c (μA)
MTJ1	$(\pi/4) \times 45 \times 90$	3.46/1.57	15.89
MTJ2	$(\pi/4) \times 64 \times 127$	1.73/0.79	31.78

Owing to the two resistance states '11' and '00' are very important to the typical two-step write method both in the conventional cell (CC) and the PC, we analyse the write current of writing the two states into cell from different previous states in this simulation, and compare the power reduction (PR) of MTJ1 between the PC and the CC. To drive the two MTJs in Table 2, an access transistor M0 with the smallest width 130 nm is required in the conventional MLC STT-RAM. Similarly, two access transistors M1 and M2 with the same smallest width 55 nm are required in the PC. As the width of M0 (130 nm) is even larger than the sum of M1 and M2 (2×55 nm), the area cost is limited obviously. The simulation results of write current, used the parameters mentioned above, are presented in Fig. 3.

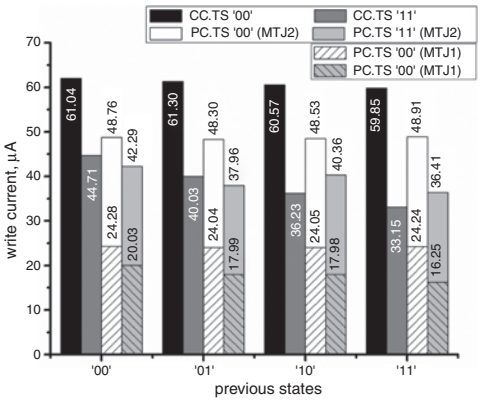

Fig. 3 *Write current of both CC and PC to switch resistance states from previous states to target states (TS)*

To compare the PR of MTJ1, we calculate percentage of the PR on MTJ1 using the formula as follows:

$$PR\% = 1 - (I_{MTJ1}/I_{MTJ2})^2 \ \% \quad (1)$$

Here two methods are used. The first method called theoretical method, I_{MTJ1} and I_{MTJ2} in the formula are the write currents of the PC are shown in Fig. 3. The second method called practical method, I_{MTJ1} and I_{MTJ2} are the write currents of the CC and the PC, respectively. The simulation results are presented in Fig. 4.

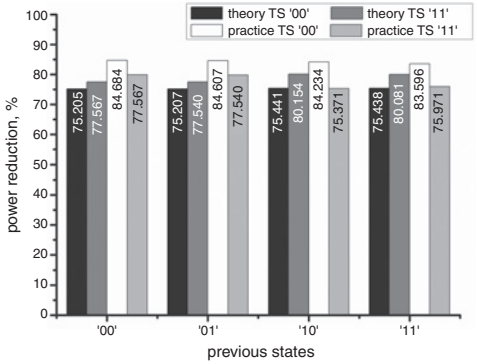

Fig. 4 *Percentage of PR on MTJ1 calculated by two methods*

Conclusion: In this Letter, we performed a detail analysis of the write current in the conventional MLC STT-RAM cell and find a huge unnecessary extra write current on MTJ1, which will lead to extra power consumption and lifetime degeneration on MTJ1. To wipe out the extra write current, a 2T2MTJ MLC STT-RAM cell is proposed here. Then we discuss the basic operations and advantages of the PC. Furthermore, to check the feasibility of the PC, a simulation is introduced. The simulation results show 77% average PR of MTJ1 with limited area cost. With the PR of MTJ1, the degeneration of lifetime will be relieved at the same time.

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