Spin-transfer torque magnetoresistive random-access memory technologies for normally off computing (invited)

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Most parts of present computer systems are made of volatile devices, and the power to supply them to avoid information loss causes huge energy losses. We can eliminate this meaningless energy loss by utilizing the non-volatile function of advanced spin-transfer torque magnetoresistive random-access memory (STT-MRAM) technology and create a new type of computer, i.e., *normally off computers*. Critical tasks to achieve normally off computers are implementations of STT-MRAM technologies in the main memory and low-level cache memories. STT-MRAM technology for applications to the main memory has been successfully developed by using perpendicular STT-MRAMs, and faster STT-MRAM technologies for applications to the cache memory are now being developed. The present status of STT-MRAMs and challenges that remain for normally off computers are discussed. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4869828]

I. INTRODUCTION

The room temperature (RT) tunnel magneto-resistance (TMR) effect[1,2] found in Al-O based magnetic tunnel junctions (MTJs) has enabled a new type of non-volatile memory, i.e., the magneto-resistive random access memory (MRAM). The concept of "*instant-on computers*" has attracted attention around 2000 as an application of MRAMs. MRAMs were expected to reduce the start-up time of computers and to reduce user frustration. MRAMs play an important role only when computers start up in instant-on computers. However, we believe that the potential of MRAMs is not limited to start up and they have hidden potential to change the computer architecture. We therefore proposed the concept of "*normally off computers*"[3] in 2001 from this point of view.

Suppose that you are typing on a keyboard. During the approximately 100 ms to move your finger from one key to the next, the computer needlessly wastes energy waiting for your input. This is because most parts of present computers are made of volatile devices, i.e., transistors and dynamic RAMs (DRAMs), which lose information when powered off. The present computers are designed on the premise that power will always be supplied, i.e., they will be *normally on*. If computers are redesigned so that power consumption is zero during any short intervals when users are absent from the job without them even being aware of it, very energy efficient computers such as mobile personal computers running on solar batteries or hand-cranked dynamos can turn into a reality.[4]

We need high performance non-volatile devices that do not require a power supply to retain information to create normally off computers and simultaneously guarantee sufficiently high speed operation to manipulate the information. The main memory, for example, requires performance as fast as 10 to 30 ns (Fig. 1) and density as high as 1 Gbit per chip. However, around 2000, the feasibility of such high density MRAMs was not clear at all. Intensive research and development of magnetic field writing MRAMs[5,6] successively led to the commercial production of MRAMs[7] in 2003, but their use has been limited to specific applications due to their small memory capacity of 8 Mb.

MRAM technologies have made marvelous advances toward main memory applications in the last decade. Spin-transfer torque (STT) magnetization switching of Al-O based

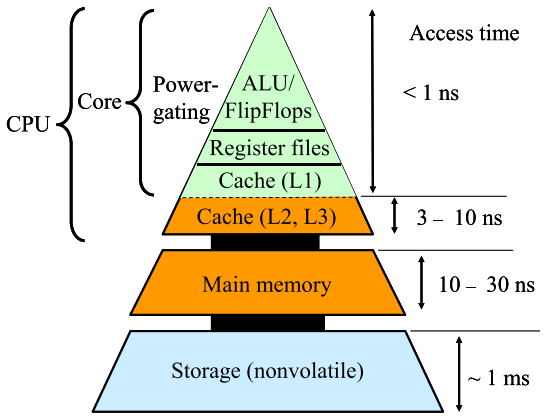

FIG. 1. Layered structure of computer systems. Typical access times for smartphone, personal computer, and supercomputer systems are shown.

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MTJs was reported[8] in 2004. Replacement of Al-O tunnel barriers with MgO enabled huge enhancements to the TMR effect[9–11] in 2004. The successive invention[12] of the CoFeB/MgO/CoFeB MTJ structure reported in 2005 was decisive in the mass production of MgO based MTJs (Fig. 2). Finally, the STT switching of perpendicular magnetization MTJs[13] was reported in 2007. These successive breakthroughs convinced us of the reality of non-volatile main memories.

However, many problems still remain to be solved to achieve normally off computers. The problems are not only limited to materials and MTJ devices but circuits, memory architectures, operating systems, and peripherals, which should also be redesigned. This paper reports our efforts to attain normally off computers and discusses the challenges that remain.[4,14,15]

II. STT-MRAMS FOR MAIN MEMORY

Although DRAMs consume more than half the power of computer systems,[4] they are presently the only devices used for the main memory because of their high levels of performance, i.e., fast operation, infinite read/write endurance, and high density.[4] Even though MRAMs have inherent advantages in faster operation and infinite read/write endurance, the feasibility of gigabit class density has not been clear until recently.

A. Spin-transfer torque switching

One of the main weaknesses of classical magnetic field writing MRAMs is that the required writing current rapidly increases with reduced MTJ size. This has prevented MRAM density from going beyond some tens of megabits. A scalable way of changing the direction of magnetization, i.e., by quantum mechanical STT magnetization switching, was theoretically proposed[16,17] in 1996, and attained in metallic magnetic multilayers[18] in 1999 and in Al-O based MTJs[8] in 2004.

B. High TMR ratio in CoFeB/MgO/CoFeB MTJs

Another problem has been the excessively low TMR ratio of Al-O based MTJs. The TMR ratio increased up to 70% until 2004 (Fig. 2), but this was almost the theoretical upper limit for Al-O based MTJs. Gigabit class MRAMs require a TMR ratio of at least 150% for reliable reading. Theoretical papers[19,20] predicted huge TMR ratios in MgO based MTJs by utilizing the coherent tunneling effect. We[9,10] and IBM[11] simultaneously accomplished these in 2004 although these MgO MTJ structures were not suitable for mass production. In 2005, we found that a combination of CoFeB electrodes and an MgO barrier layer was suitable for mass production.[12] CoFeB/MgO/CoFeB MTJs are currently standard read heads for hard disk drives.[21]

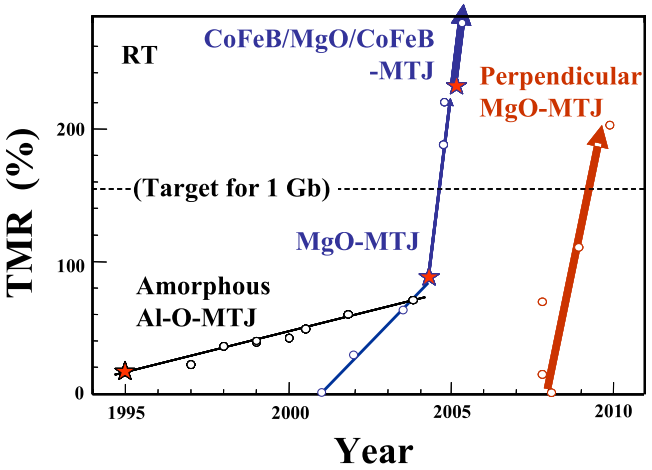

FIG. 2. Increase in TMR ratio of MTJs by year.[14,21] Stars indicate first reports of room temperature TMR,[1,2] TMR higher than that of Al-O MTJs,[9] and CoFeB/MgO/CoFeB MTJs.[12]

The combination of STT switching and CoFeB/MgO/CoFeB MTJs enabled the first integration of STT-MRAMs[22] in 2005. Evespin announced the commercialization of 64 Mb STT-MRAMs in 2012.

C. Perpendicular STT-MRAMs

The design rule of MTJs for gigabit class MRAMs should be smaller than 30 to 40 nm. Limited electrical current from such small transistors requires the STT-switching current to be less than 50 μA and the current density to be less than 1 MA/cm^2. The direction of magnetization should simultaneously be tightly fixed against thermal agitation to preserve the information for more than 10 years. This corresponds to energy barrier ΔE between two stable states with opposite magnetization directions being typically larger than 60 k_BT, where k_B is the Boltzmann constant and T is the ambient temperature. Theoretical expressions of the critical current, I_{c0}, are[23]

$$I_{c0}(\text{perpendicular}) = 4\pi e\alpha[2\,\Delta E]/hg \tag{1}$$

and

$$I_{c0}(\text{in-plane}) = 4\pi e\alpha[2\,\Delta E + 2\pi {M_s}^2 tF^2]/hg, \tag{2}$$

where e, α, h, g, M_s, and t correspond to the electron charge, damping constant, Planck's constant, spin-transfer efficiency, saturation magnetization, and thickness of an information storage layer. These two equations indicate that smaller I_{c0} can be expected for perpendicular MTJs (p-MTJs) if the parameter values are the same. The second term in Eq. (2) is the diamagnetic term, and it reflects the fact that the trajectory of magnetization motion by STT in in-plane MTJs is out of the film plane.[23,24] The second term is typically one order larger than the first term.

The origin of the ΔE of in-plane MTJs is weak electromagnetic anisotropy of the elliptical cell shape, which makes the memory cell area around $10F^2$ where F is the feature size. In contrast, the ΔE of p-MTJs derives from strong quantum mechanical anisotropy that originates from the anisotropic arrangement of atoms. Therefore, p-MTJs can be circular, and the cell area can be as small[14] as $6F^2$. Large perpendicular magnetic anisotropy is also beneficial to provide a large ΔE for a small bit.

Perpendicular STT-MRAMs are very attractive for high density memories. However, at 2006, there were no reports of STT switching in p-MTJs. Only data with perpendicular giant magneto-resistive (GMR) devices had been

reported,[23,25,26] but their current densities were huge (Fig. 3). Furthermore, it had been believed to be too difficult to apply *p*-MTJs to STT-MRAMs because large perpendicular magnetic anisotropy inevitably increases damping factor α in Eq. (1), resulting in increased writing current. In 2007, we reported the first demonstration of STT switching in *p*-MTJs by using the structures of *p*-CoFeB/MgO/*p*-CoFeB MTJs sandwiched between magnetic metals with high perpendicular anisotropy such as TbFeCo.[13] As expected, the *p*-MTJs demonstrated low current and fast STT switching with high thermal stability.[27] We successively reduced the STT switching current density to below 1 MA/cm^2 by 2010 (Fig. 3). These achievements definitively changed the research trend of STT-MRAMs. STT switching in *p*-MTJs was also reported by other groups[28,29] in 2010.

III. STT-MRAM FOR CACHE MEMORY

Central processing units (CPUs) are composed of core and last level caches (LLCs), i.e., L2 and L3 (and L4) caches (Fig. 1). The main power consumer of these components of CPUs are LLCs because most transistors inside CPUs are used for static RAMs (SRAMs) for LLCs. LLC capacity depends on the purpose of use and typically ranges from 1 to 100 MB. Individual SRAMs waste static power irrespective of whether jobs are present because leakage current flows through transistors as long as power is supplied. SRAM is "normally on type memory cell" design. Because larger cache capacities very effectively enhance CPU performance, there is strong demand for smaller SRAMs. However, smaller transistors induce larger leakage current. The power consumed by leakage current is the most serious problem in designing high performance processors.

Analysis of SRAM based cache memory operation shows that LLC has very short standby time from 10 ns to 100 ns while CPU is active.[30] For this standby time, more than 80% energy is consumed of the total cache memory energy. The most effective way to eliminate leakage is to use a new memory cell deign with "normally off type".

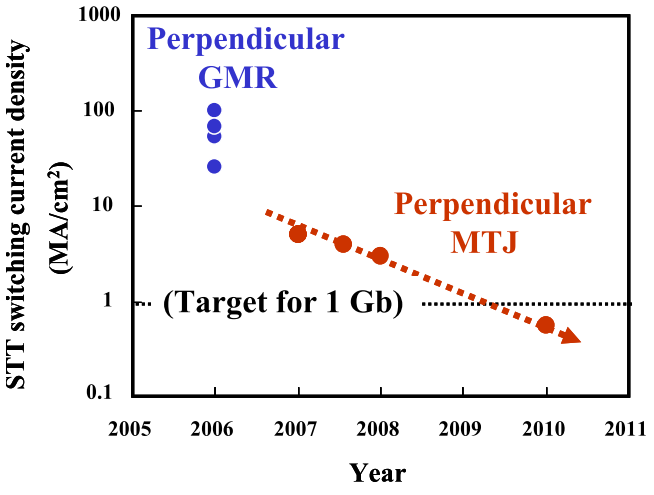

FIG. 3. History of reduction in STT switching current density of perpendicular GMR[23–26] and MTJs.[14]

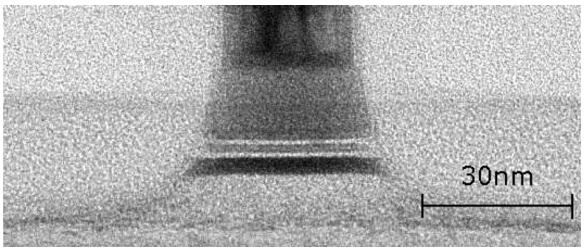

FIG. 4. Transmission electron microscope image of perpendicular MTJ.

Although MRAMs are free from power consumed by leakage current, their speed, which was developed for main memory applications, is too slow for cache memory applications. The clock frequency of CPUs for smartphones, tablets, personal computers, and super computers typically ranges from 1 to 5 GHz. LLCs in such high performance CPUs need access speeds of 3 to 10 ns (Fig. 1).

A. Fast and low power STT switching in p-MTJs

The I_{c0} for STT switching increases with reduced writing pulse width especially below 10 ns because the switching mode changes from being thermally activated to being precessional.[22,31] We need new *p*-MTJs that switch rapidly with low current, high ΔE, and high TMR ratios. We recently succeeded in demonstrating 3-ns-pulse STT switching[32] at 50 μA in a sub-30-nm size *p*-MTJ (Figs. 4 and 5). The programming energy was 90 fJ, which is the smallest value ever reported for such high speed operation. The compact size of the MTJ and its small α of 0.004 were keys to reducing the current (Eq. (1)). A ΔE of 61 k_BT and a TMR ratio of 150% were obtained.[32,33]

B. Fast reading

Fast and low power STT switching *p*-MTJs are crucial but not sufficient to replace the SRAMs for LLCs with STT-MRAMs. The cell structure and read/write circuits should also be redesigned. A typical example is the read speed. The conventional current sensing circuit with the 1T-1MTJ cell structure used for STT-MRAMs for main memory applications cannot read out information faster than 10 ns. We adopted a current-integral sensing scheme and differential

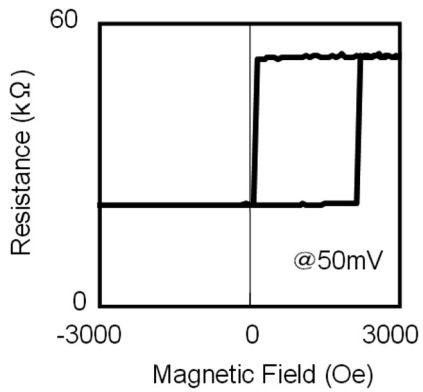

FIG. 5. TMR ratio of 150% was obtained in perpendicular MTJ.

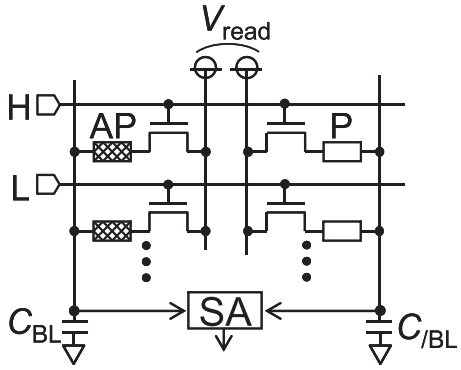

FIG. 6. Pair of 1T-1MTJ complementarily stores one bit. Sense amplifier (SA) differentially detects voltage of bit line capacitors for fast reading.

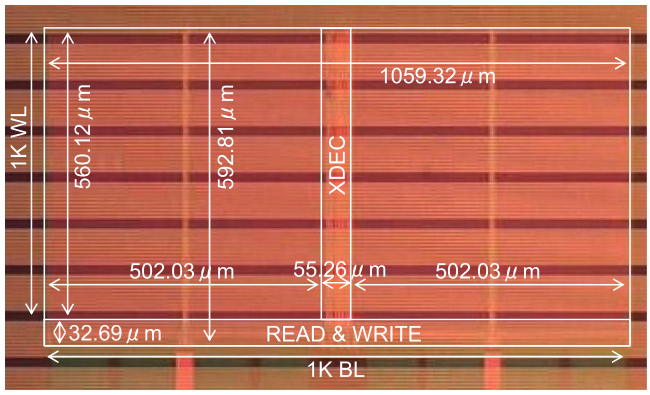

FIG. 7. Chip surface photo for embedded cache memory with dual 1T-1MTJ cell STT-MRAM fabricated in 65 nm CMOS process. MTJ arrays were fabricated on the top surface of this chip to measure circuit performance.

amplification using dual 1T-1MTJ cell structures (Fig. 6) to increase the read speed without increasing power, and achieved 4-ns reading speed.[33] The cell size of a dual 1T-1MTJ cell is 0.45 μm^2 with standard 65-nm CMOS process rule, which is much smaller than that of a standard SRAM. It could be less than 0.2 μm^2 with specific MRAM process rule. The LLC capacity can be increased without increasing the chip size, and larger LLC capacity enables faster I/O speed than an SRAM.

C. Energy saving and performance of *p*-MTJ based LLC

A 1-Mb STT-MRAM macro with a cell efficiency of over 75% was designed and fabricated with a 65-nm CMOS process (Fig. 7). It was possible to achieve read operation with a 4-ns cycle time at a core voltage of 1.05 V. The estimated read power consumption with 256-bit I/O width was 17.8 mW and that for write was 46.5 mW.[33]

The power and performance of the L2 cache with a dual 1T-1MTJ cell STT-MRAM structure were evaluated with a simulation based on gem5 by assuming a variety of computer uses. The assumed CPU core was a 1-GHz ARMv7-a single core architecture with a 64-KB SRAM based L1 cache. The processor simulations were conducted with Standard Performance Evaluation Corporation (SPEC) CPU2006 benchmarks.[30] Our dual 1T-1MTJ cell based L2 cache, compared to the typical 0.8 V operating SRAM design, could reduce the energy per instruction (EPI) by 64%, while maintaining instructions per cycle (IPC) performance degradation within 6% (Fig. 8). Note that our dual 1T-1MTJ cell is a typical normally off type. Therefore, not only during CPU standby time but also during CPU active time, consumed power can be largely and effectively saved. The EPI and IPC evaluated for other STT-MRAMs previously reported[34–36] are also given in Fig. 8. Except for our advanced cache cell structure, the use of STT-MRAMs in LLCs usually increases energy consumption as opposed to what is expected. This means that advanced *p*-MTJs and advanced cell structure designs are critical for normally off computers.[30,37,38]

IV. CPU CORE

A. Dilemma with non-volatile memories

The processor core is composed of an arithmetic logic unit (ALU), flip-flops, register files, and an L1 cache (Fig. 1). Can we also expect the benefits of STT-MRAM technology to flow to the core? Because all components in the core are located near the ALU, their access to the information should be very frequent and very fast (<1 ns). All

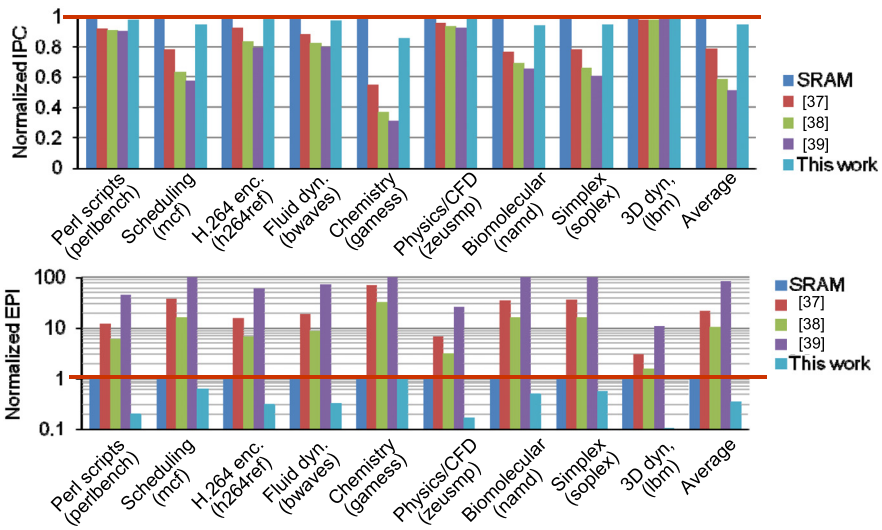

FIG. 8. Comparison of IPCs and EPI for 1-Mbit L2 caches made with different cell structures.[34–36] Our dual 1T-1MTJ cell enables EPI improvements of more than 64% with degraded IPC of less than 6%. Redrawn from Ref. 33.

components of the core are made of transistors whose speed can be as fast as 1 ps and whose operation energy can be as low as 0.1 fJ to satisfy these requirements. Our *p*-MTJ[32,33] with 3 ns and 90 fJ is presently the most advanced available, and its performance can hopefully be improved by one order of magnitude in the future. Nevertheless, we still cannot deny that the active performance of STT-MRAMs is far inferior to that of volatile transistor circuits in the core. The core also suffers from static power loss due to leakage current through the transistors in addition to active power loss. The implementation of STT-MRAMs into L1 caches, registers, and logic circuits can eradicate static power. However, a STT-MRAM simultaneously drastically increases the active power in the core and completely negates the reduction in static power. This is what we call the "*dilemma of non-volatile memory*,"[4] which has already been noticed in LLCs, and it explains why some STT-MRAM based caches waste much more power than conventional SRAMs (Fig. 8). The boundary for the superiority of STT-MRAMs against SRAMs with our advanced cache cell lies between L1 and L2 caches (Fig. 1). Although further improvements to the performance of *p*-MTJs and circuit design will push the boundary upward into the L1 cache (Fig. 1), as long as the STT mechanism is used, most of the L1 cache will need to be comprised of conventional SRAMs. The implementation of STT-MRAMs for registers, flip-flops, and logic circuits will be much harder.

B. Combination of STT-MRAM and power gating

Normally off processor cores have already been commercially available since 2007, which has been achieved with power gating technology. There is a small amount of information inside the core, and the circuit speed is fast. Therefore, when there are no jobs, the core copies its important information bits into the cache memories, and the core powers off except for the limited information retained in the cache memories. When a job appears, the core turns on the power and copies back the stored information to resume the job. This series of actions takes about 100 μs, and users never notice it. Power gating technology was introduced into commercial processors around 2007, e.g., Intel Core 2, and has now been adopted by all CPUs. Power consumption per performance by the core has been drastically reduced.

Because power gating is not effective for manipulating huge amounts of information, its use is mostly limited to the core. Non-volatile STT-MRAM and power gating technologies converge at the L1-LLC boundary. The combination of these two technologies is important to further increase power efficiency for both L1 and LLCs. Since memory cell arrays with normally off type design do not need power gating, very fast and effective power gating can be conducted only for logic parts in the cache memories. In order to extract the full potential of STT-MRAMs, collaboration with the field of computing science has become essential.

C. New non-volatile spintronic devices

Power gating is an effective technology to increase the power efficiency of the core. However, its implementation needs extra circuits and complex process management. As previously described, the boundary to implement non-volatile devices strongly depends on their performance. Non-volatile spintronic devices whose active power is much lower than that of STT-MRAMs are urgently required to expand the boundary and to evolve computer systems. Transistors have evolved from current driven bipolar transistors to voltage driven field-effect-transistors to improve their power efficiency. The change to voltage driven magnetization switching is one of the most promising paths to lower power consumption as has been suggested by the history of transistors.

Controlling the magnetic anisotropy of metallic magnetic thin films (FePt and FePd) by applying voltage through liquid electrolyte[39] was reported in 2007. In 2009, we demonstrated control of the magnetic anisotropy of Fe and FeCo films with voltage in device structures that were entirely solid state.[40] We further succeeded in demonstrating fast ($\sim$0.4 ns) voltage-induced precessional magnetization switching in an Fe/MgO/FeCo structure.[41]

Although it is presently too early to judge the feasibility of new spintronic devices for the core, recent advances in spintronic technologies are very encouraging.

V. OTHER APPLICATIONS

In real high-end computer systems, a variety of peripheral circuits and devices are needed in addition to the architecture outlined in Fig. 1. Data access frequency is low and fast operation speed is not required because they are located far from the processor core. There are also low-end processors that are not required to be so fast as high-end ones. Some devices such as configuration data memory for field-programmable-gate array (FPGA) and one-time-programmable memory for securing data do not need fast operation.[42] Restrictions imposed by the dilemma become less stringent for such devices. The standby-power free advantage of STT-MRAM based non-volatile logic, for example, will find a variety of applications such as in sensor-network and healthcare systems.

However, being free from the dilemma simultaneously means that the most important advantages of STT-MRAMs are lost, i.e., fast read/write speeds and infinite endurance against other types of non-volatile devices such as ferroelectric RAMs, phase change RAMs, resistive RAMs, and flash memories. Non-volatile logic devices based on these non-volatile memories are already commercially available.[43] STT-MRAM based logic devices are required to demonstrate better cost performance against rivals. Once the mass production process for STT-MRAMs for main memory applications is established, it can easily be diverted to lower performance STT-MRAM based circuits. That will provide them with excellent cost performance.

We also need to develop normally off displays because displays in computer systems typically consume 20%–40% of the power of the systems.[4] Although STT-MRAMs will not play important roles in displays, a variety of normally off type displays, such as electrostatic paper displays and

micro-electro mechanical systems (MEMS) displays, are currently being developed.

VI. CONCLUSIONS

The concept and technical requirements for normally off computers were discussed. Spintronics based normally off computers have not yet been introduced 12 yr after the concept was first proposed. However, marvelous advances made in the last decade and collaboration with the field of computing science are now making normally off computers a reality.

ACKNOWLEDGMENTS

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