

Self-referenced multi-bit thermally assisted magnetic random access memories

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The feasibility of 3-bits per cell storage in self-referenced thermally assisted magnetic random access memories is demonstrated both by macrospin simulations and experiments. The memory dot consists of a storage layer where CoFe/CoFeB magnetization direction is pinned by an IrMn layer using the ferromagnet/antiferromagnet interfacial exchange coupling, separated by an MgO tunnel barrier from a CoFeB sense layer whose magnetization direction is free to rotate. Writing is performed by heating the antiferromagnet above its blocking temperature by sending a current pulse through the magnetic tunnel junction, with the application of an in-plane field during the subsequent cooling phase, thus setting the new storage layer pinning direction. This pinning direction actually carries the information stored in the storage layer. Reading is performed by applying a rotating field, inducing a coherent rotation of the sense layer, and subsequently locating the field angle associated with the minimum measured resistance. This angle corresponds to the parallel magnetic configuration of the magnetic tunnel junction and therefore allows determining the pinning direction established during the write operation. The number of distinguishable pinning angles defines the total number of bits that can be stored in a single dot. © 2014 AIP Publishing LLC.

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Spinelectronics, merging magnetism and electronics, has kept growing in the past 20 yr thanks to a strong synergy between fundamental research¹ and applied developments,² especially in the fields of magnetic storage (hard disk drives) and memories (Magnetic Random Access Memory (MRAM)). MRAMs based on magnetic tunnel junctions are nowadays receiving an increasing interest within the microelectronics industry due to their unique combination of non-volatility, write/read speed (~ 30 ns or below), endurance ($> 10^{16}$ cycles), density and radiation hardness.³ In particular, spin transfer torque MRAM has been identified⁴ in the International Technology Roadmap for Semiconductors (ITRS) as one of the two most promising technologies of non-volatile emerging memories (with RedOx RAM⁵) allowing down size scalability to the 22 nm technology node and beyond.

While MRAM products based on Toggle-Switching⁶ are already available, another generation based on thermally assisted writing is under development.⁷ Thermally-assisted MRAM (TA-MRAM) exploits the temperature dependence of ferromagnet/antiferromagnet interfacial exchange coupling to overcome the write consumption versus thermal stability dilemma usually observed in magnetic recording technologies. High stability at operating temperature is obtained by pinning the storage layer's magnetization with an antiferromagnet by the exchange bias coupling occurring at their interface. Writing occurs through a thermally assisted scheme. When heated above the antiferromagnet's blocking

temperature, the ferromagnetic layer becomes free, and its magnetization can be set by a magnetic field. The heating (at about 250 °C) is generated by current flowing through the magnetic tunnel junction (MTJ). Simultaneously, a magnetic field switches the ferromagnetic layer in the desired direction. The heating is then stopped, the junction cools down under the applied magnetic field that maintains the storage layer magnetization in the appropriate direction. Exchange coupling is re-established, pinning the storage layer in the new direction. Selectivity is achieved in TA-MRAM by the combination of heating and magnetic field.⁸ In self-referenced TA-MRAM, the pinned reference layer is replaced by a soft switchable reference layer,⁹ referred as the sense layer (Figure 1). This opens wide application prospects due to their in-stack combination of memory and logic (XOR) functions,¹⁰ including multi-bit storage.¹¹ The multi-bit storage capability gives increased storage densities

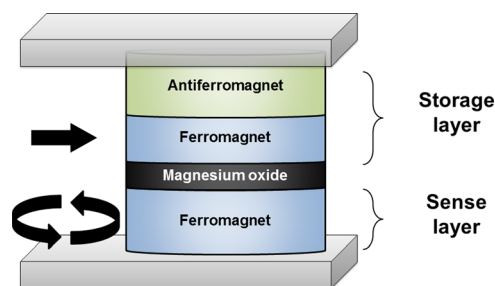


FIG. 1. Schematic of a self-referenced MRAM for multi-bit applications. The black arrows denote the sense and storage layer magnetizations during a reading operation.

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without requiring moving to smaller and more technically challenging technology nodes.

This paper reports the demonstration of feasibility of 3-bits per cell storage obtained in self-referenced MRAM cells. The readout is based on the phase of the oscillation of resistance produced by a 360° rotation of the sense layer magnetization. The concept was explored by macrospin simulations and demonstrated experimentally on cells of various diameters down to 110 nm.

Instead of reading a resistance level, as in TA-MRAM, or a change in resistance, as in regular self-referenced MRAM, multi-bit self-referenced TA-MRAMs exploit the full resistance response obtained as the sense layer aligns itself with an external rotating field. During this field rotation, the MTJ resistance continuously varies as a function of the field angle (see Figure 2), reaching a maximum (respectively, minimum) value when the sense and storage layers moments become antiparallel (respectively, parallel). Thus, the data, stored in the storage layer magnetization direction, can be read out from the phase of this oscillatory resistance, for instance, by an external digital signal processor.

Therefore, to achieve n -bits per cell storage, the storage layer must be writable in at least 2^n distinct directions. Unlike resistance-level-based multi-bit operations in MRAM reported in previous works,¹² this operation does not rely on a series of predefined resistance levels, but rather on the angular position of a minimum of resistance. It is therefore more tolerant to process related cell to cell variability such as size or resistance per area variations, though at the expense of a more complex readout mechanism.

3-bits per cell storage was first assessed by macrospin simulation and then confirmed by experimental results. In order to simulate the behaviour of a multi-bit self-referenced MRAM, a macrospin approach based on the Stoner-Wohlfarth¹³ model of magnetization reversal was developed. Under the assumption that both the sense and the storage layers magnetizations behave like macrospins, the system energy E is written¹⁰

$$E = -H[m_1 \cos(\theta_1 - \theta_H) + m_2 \cos(\theta_2 - \theta_H)] - \frac{H_{K_1} m_1}{4} \cos(2\theta_1 - 2\theta_{K_1}) - \frac{H_{K_2} m_2}{4} \cos(2\theta_2 - 2\theta_{K_2}) + \frac{H_{1 \rightarrow 2} m_2 + H_{2 \rightarrow 1} m_1}{2} \cos(\theta_1 - \theta_2) - H_{exch} m_1 \cos(\theta_1 - \theta_P), \quad (1)$$

where H and θ_H are the external field amplitude and its direction with respect to the easy axis of the layers, $m_{1(2)}$, $\theta_{1(2)}$, $H_{K_{1(2)}}$, and $\theta_{K_{1(2)}}$ are the moment, moment angle with respect to the easy axis, uniaxial anisotropy field, and easy axis angle, respectively, of the storage (1) and sense layer (2). $H_{1 \rightarrow 2}$ and $H_{2 \rightarrow 1}$ are the dipolar fields generated by the storage layer on the sense layer and the other way around. H_{exch} and θ_P are the ferromagnet/antiferromagnet exchange coupling field and the angle characterizing the pinning direction. All fields are expressed in Oe and all moments in emu. Energy minimization was performed using a conjugate-gradient based algorithm. The resistance R of the MTJ was calculated using¹⁵

$$R = \frac{\bar{R}}{1 + \frac{TMR}{2} \cos(\theta_1 - \theta_2)}, \quad (2)$$

where TMR is the tunnel magnetoresistance. Figure 2 shows experimental data fitted with (2), the results being consistent with previous works.^{14,15}

Simulation of the write operation is performed by applying an adequate external field profile and cancelling the exchange bias term in the energy function before minimizing it, thereby emulating a heating voltage unpinning the storage layer. Assuming that both layers have the same anisotropy amplitude and direction (i.e., $H_{K_1} = H_{K_2} = H_K$ and $\theta_{K_1} = \theta_{K_2} = 0$), using Sylvester's criterion to infer the positive definiteness of the energy Hessian matrix,¹⁶ indicating a stable configuration, it is possible to deduce the analytical expressions of the field requirement for both the read and the write operation to have the sense and storage layers aligned along the field

$$H_{write} = H_{1 \rightarrow 2} + H_{2 \rightarrow 1} + H_K, \\ H_{read} = \frac{H_{1 \rightarrow 2} + H_{2 \rightarrow 1} - H_{exch}}{2} + H_K + \sqrt{\left(\frac{H_{1 \rightarrow 2} - H_{2 \rightarrow 1} + H_{exch}}{2}\right)^2 + H_{1 \rightarrow 2} H_{2 \rightarrow 1}}. \quad (3)$$

The experimental data were obtained on IrMn/CoFe/CoFeB/MgO/CoFeB MTJ patterned into cylindrical pillars of various diameters ranging from 110 nm to 1000 nm. Electrical characterizations were performed on an automatic wafer tester with two orthogonal field generating coils. Heating voltage pulses were applied across the MTJ under a constant field set at 8 distinct angles, and whose amplitudes were set from 100 Oe to 600 Oe. Reading was then subsequently performed using a rotating field of amplitude equal to that used for writing.

The pinning angles of the storage layer magnetization inferred from the phase of the resistance responses are plotted in Figure 3 as a function of the write field

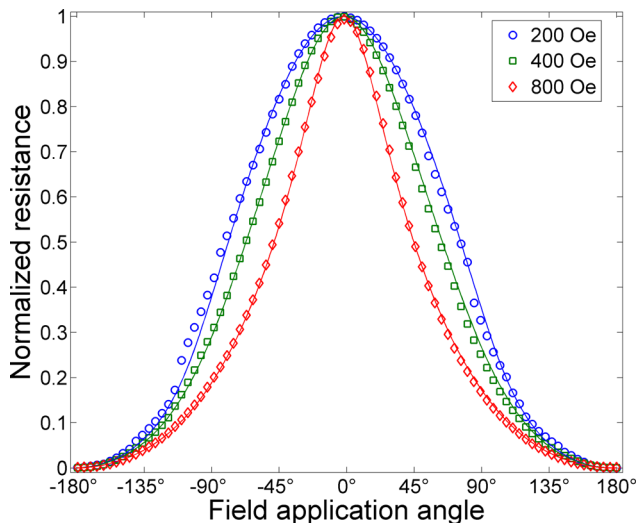


FIG. 2. Experimental (dots) and simulated (solid line) resistance responses of a $1 \mu\text{m}$ self-referenced MRAM cell under a circular field pattern of various amplitudes. The fits were obtained using a single set of simulation parameters ($H_{K_1} = H_{K_2} = 50$ Oe, $H_{exch} = 700$ Oe, $\theta_{K_1} = \theta_{K_2} = 0$, and $\theta_P = -2.5^\circ$).

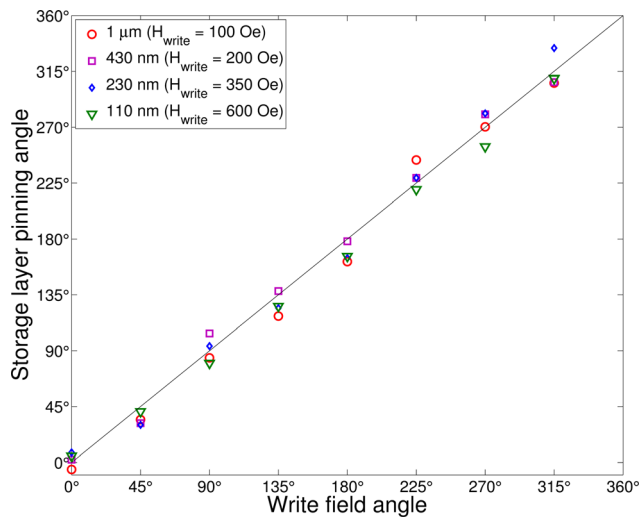


FIG. 3. Measured pinning angle of the storage layer as a function of the write field angle, for 8 writing directions and various MTJ diameters. The continuous line denotes the result expected from the macrospin simulation.

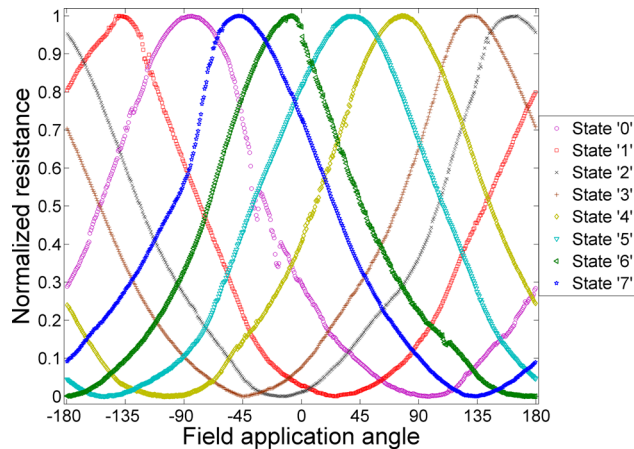


FIG. 4. Normalized resistance as a function of the field angle (applied field = 600 Oe) measured on a 110 nm wide self-referenced MRAM cell written in 8 directions, demonstrating a 3 bits per cell device feasibility.

application angle. Within the range of write field investigated ($H_{\text{write}} > H_{1 \rightarrow 2} + H_{2 \rightarrow 1} + H_K$), the storage layer magnetization is asymptotically aligned to the applied write field direction within 5° . Lower values of write field would result in the storage layer magnetization being aligned in-between its intrinsic anisotropy axis and the write field angle, leading thus to a write error (not shown).

The normalized responses during the read operation for the 110 nm MTJ are plotted in Figure 4 and confirm the feasibility of 3 bits functionality at that dimensions. Some

deviation from the model and noise can be observed on the experimental data (Figures 2 and 4), which are ascribed to micromagnetic distortions at the edge of the pillars likely associated with imperfections in the pillar shapes arising from the etching process.

In order to further reduce the reading and writing consumption of the device, both the read and write field requirements need to be reduced. To do that, the magnetostatic interaction ($H_{1 \rightarrow 2} + H_{2 \rightarrow 1}$) between both layers has to be minimized. This can be achieved by either using low magnetization materials or synthetic antiferromagnet bilayers that reduce magnetostatic interactions thanks to magnetic flux closure within each bilayers.

In summary, a functional 3 bits self-referenced MRAM has been successfully demonstrated both by simulation using a Stoner-Wohlfarth model and experimentally on MTJ of various dimensions down to 110 nm. Further studies should be conducted in order to enhance the scalability of read and write fields and reduce power consumption. For that purpose, either synthetic antiferromagnet structures or low-magnetization-ferromagnets could be employed for a significant reduction of magnetostatic interactions between the storage and the sense layers.

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