# Mechanism of power consumption inhibitive multi-layer Zn:$SiO_2$/$SiO_2$ structure resistance random access memory

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In this paper, multi-layer Zn:$SiO_2$/$SiO_2$ structure is introduced to reduce the operation power consumption of resistive random access memory (RRAM) device by modifying the filament formation process. And the configuration of multi-layer Zn:$SiO_2$/$SiO_2$ structure is confirmed and demonstrated by auger electron spectrum. Material analysis together with conduction current fitting is applied to qualitatively evaluate the carrier conduction mechanism on both low resistance state and high resistance state. Finally, single layer and multilayer conduction models are proposed, respectively, to clarify the corresponding conduction characteristics of two types of RRAM devices. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4843695]

## I. INTRODUCTION

For next generation nonvolatile memory,[1–7] the resistance random access memory (RRAM) was widely discussed and investigated recently due to its superior properties such as low cost, simple structure, fast operation speed, and non-destructive readout.[8–13] Among numerous resistive switching materials, the silicon-based oxide thin films were intensively investigated for the applications in RRAM for portable electrical devices owing to its compatibility in integrated circuit (IC) processes and relative stability compared with metal oxide materials.[14–26]

Filament formation and rupture is considered to be the reason of resistive switching in RRAM devices.[27–29] Thus, the filament shape and formation process affects the magnitude of working current, which in turn influences the power consumption of the device. Meanwhile, low power consumption has always been one target of the semiconductor industry not only for the commercial interests but also for the capability of high density integration. The formation process of filament has great impact on the RRAM switching and operating properties. And it can be modified by adjusting the thickness of switching layer, types of dopants, ways of electrical operation, etc.[30–33] In this paper, multi-layer stacking technology is applied to modify the filament formation process.

Contemporary binary oxide materials have been reported having low-power RRAM switching properties by different types of structures and electrical operation.[34–36] But worldwide researchers mainly focus metal oxide system like $HfO_x$,[34] $TiO_x$,[35] and $TaO_x$.[36] By reducing the device dimension and tuning the dopant concentration, we can achieve low operation voltage in metal oxide based RRAM devices. However, most power-saving operations are based on the strictly control of compliance current or the low operation voltage is the intrinsic material property, and if the compliance current is not restricted severely, the device will suffer unrecoverable hard breakdown. Here in this research, we focus zinc doped silicon oxide RRAM owing to the relative mature background of zinc, especially in the fabrication of thin film transistor display[37–43] and the wide applied low-cost silicon oxide. Multilayer structure RRAM device is fabricated to evaluate the merits of multi-layer stacking technology in the cycling process, from which obvious reduction of operating current can be observed even the compliance current is 10 mA. Conduction current fitting combined with varied temperature measurement are used to investigate the resistance switching mechanism. Finally, single layer and multilayer conduction model are proposed to clarify the switching characteristics and the reason of working current reduction.

## II. EXPERIMENTAL DETAILS

In this study, zinc doped $SiO_2$ (Zn:$SiO_2$) by magnetic co-sputtering at room temperature is taken to form the multi

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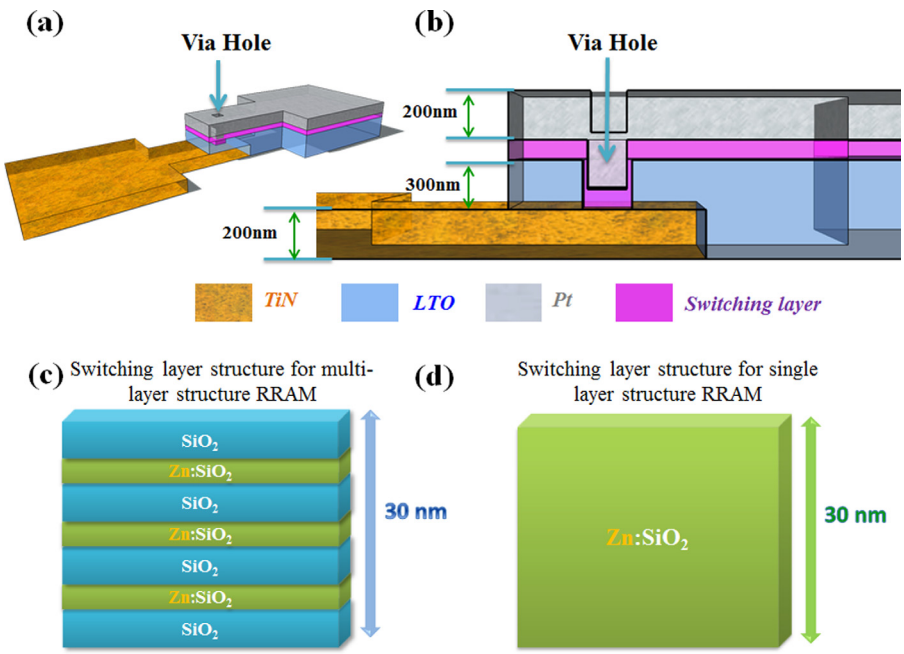


FIG. 1. Device schematic structure of (a) whole view (b) cross sectional view. (c) and (d) are the corresponding switching layer structure for multi-layer and single-layer RRAM. The switching layer is marked with purple in Figure 1(b).

resistance switching layer $Zn:SiO_2/SiO_2$ structure. To make comparison, single $Zn:SiO_2$ layer device is also fabricated. To the multi-layer Metal-insulator-metal (MIM) capacitor structure, each $Zn:SiO_2$ thin film layer is deposited by sputtering pure $SiO_2$ and Zn targets in argon ambient (4 mTorr) on a patterned $TiN/Ti/SiO_2/Si$ substrate. To the patterned substrate, The 200 nm TiN is deposited as bottom electrode and it is processed with standard lithography process to form T-shape bottom electrode. Then 300 nm low temperature silicon oxide (LTO) is grown on the whole wafer and etched to expose TiN bottom electrode and form via, in which switching layer is deposited. After the etching process, photoresist (PR) is spin-coated and etched to expose the via and the area where switching layer and top electrode will be deposited. The whole view and cross-sectional view of the device are shown in Figs. 1(a) and 1(b). The total film thickness of the active layer in the via is 30 nm and the corresponding thickness of each layer for multi-layer sample is marked out in Fig. 1(c). The single layer device is fabricated with the same parameter as the $Zn:SiO_2$ layer in multilayer sample and the thickness of switching layer is also 30 nm (Fig. 1(d)). Then, the top electrode is made of Pt by sputtering with a thickness of 200 nm on multi-layer sandwich structure. Finally, the electrical device cells were fabricated through lithography and lift-off techniques. The device area is 1 $\mu$m × 1 $\mu$m and the whole electrical measurements on single layer $Zn:SiO_2$ and multi-layer $Zn:SiO_2/SiO_2$ RRAM devices are done by Agilent B1500 semiconductor parameter analyzer.

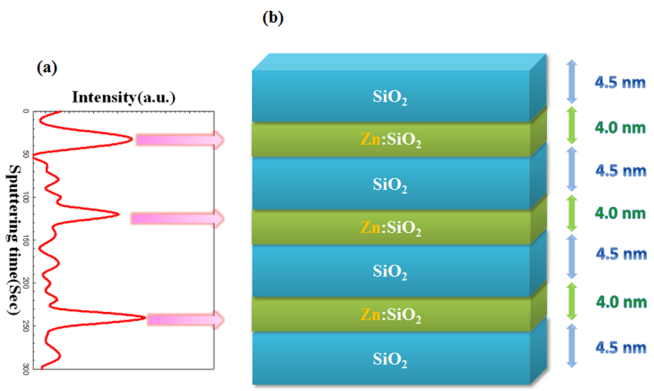


FIG. 2. Auger electron spectrum for multi-layer $Zn:SiO_2/SiO_2$ structure.

## III. RESULTS AND DISCUSSION

To verify the structure configuration of multi-layer $Zn:SiO_2/SiO_2$ film, Auger Electron Spectroscopy (AES) is applied to obtain the zinc AES spectra, which is shown in Fig. 2(a). From the AES spectra, the 7-layer stacking structure is corroborated by zinc peaks distribution.

After AES analyzing, Fourier transform infrared spectroscopy (FTIR) is used to investigate the chemical bonding of the $Zn:SiO_2$ film. Fig. 3 shows that the Si-O-Zn stretch bonding is found in the $Zn:SiO_2$ film at 1132 $cm^{-1}$. In addition, the anti-symmetric stretch mode and the symmetric

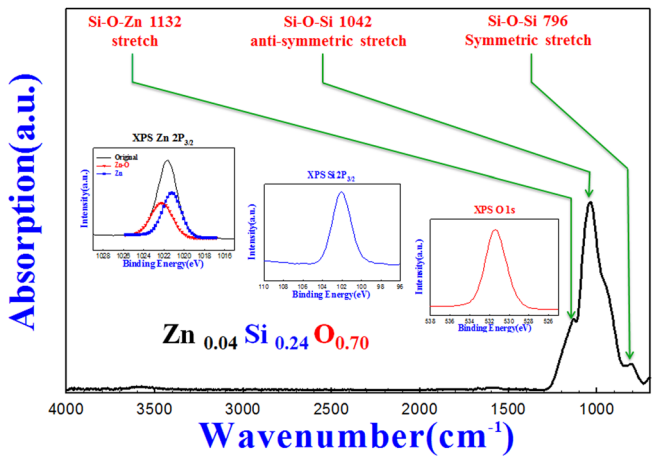


FIG. 3. FTIR spectra of $Zn:SiO_2$ film measured in middle infrared region. The XPS spectra of Zn $2P_{3/2}$, Si $2P_{3/2}$, O 1s core levels in $Zn:SiO_2$ film are shown in the insets, respectively.

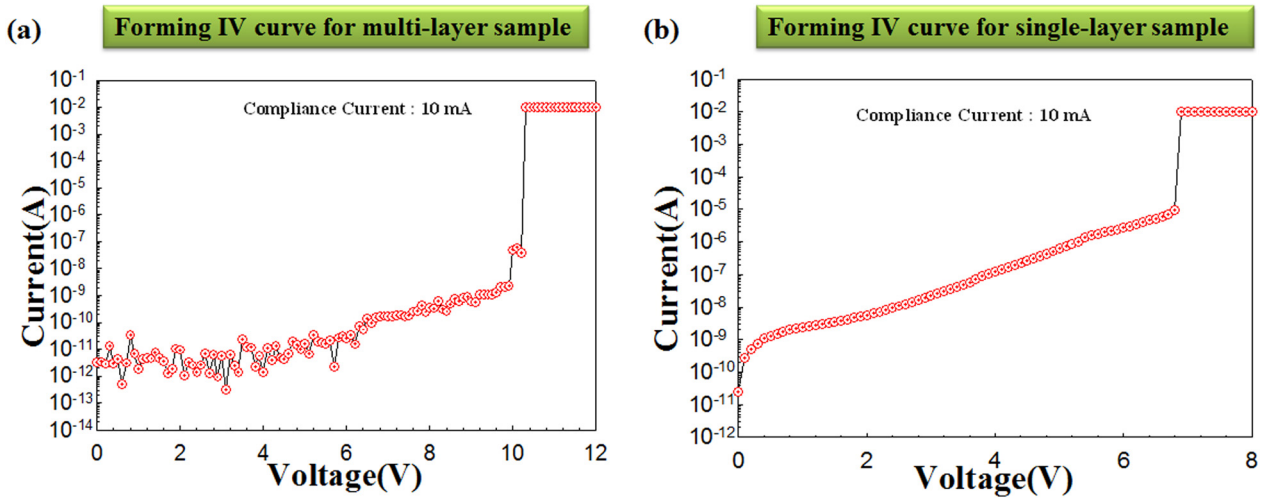


FIG. 4. (a) and (b) are the forming curve of multi-layer and single-layer devices.

stretch mode of Si-O-Si bonds are discovered at 1042 $cm^{-1}$ and 796 $cm^{-1}$, respectively. To further analyze the chemical composition of Zn:$SiO_2$ film, X-ray photoelectron spectroscopy (XPS) of Zn $2P_{3/2}$, Si $2P_{3/2}$, and O 1s peaks are performed and shown as the insets in Fig. 3. The mole fraction of Zn:Si:O in the Zn:$SiO_2$ film was 4.9%:24.9%:70.2%. Furthermore, compared with the areas of deconvolution peaks of Zn $2P_{3/2}$ core levels, we find the mole fraction of ZnO:Zn was 45.1%:54.9% in Zn:$SiO_2$ film.

After material analysis confirmation, electrical measurements are performed to investigate the performance of both types of devices. Before current-voltage sweeping, all the devices are activated by electro-forming process with a compliance current of 10 mA, as shown in Figs. 4(a) and 4(b). After that, DC sweeping is applied to analyze the standard RRAM resistive switching behavior. Fig. 5 shows the bipolar switching behavior of single Zn:$SiO_2$ layer and multi-layer Zn:$SiO_2$/$SiO_2$ structure RRAM devices by applying bias on TiN bottom electrode (inset of Fig. 5). Compared with single layer RRAM devices, it can be observed that multi-layer structure devices exhibit lower operation current on both low resistance state (LRS) and high resistance state (HRS). If the reading voltage is set with 0.1 V, the corresponding current is 300 $\mu$A in LRS and 20 $\mu$A in HRS.

To better understand the properties of both types of devices, we apply conduction current fitting, as shown in Figs. 6 and 7. Insets of Figs. 6 and 7 are their corresponding fitting curve. From Fig. 6, we can find that the HRS of single layer devices exhibit Poole-Frenkel conduction mechanism owing to the existence of defects between ruptured filament and bottom electrode, which act as the conduction media of HRS leakage current. Nevertheless, the HRS of multi-layer devices also reveal Poole-Frenkel conduction mechanism, and this is ascribes to the carrier transfer through the heterojunction defects produced between zinc extended-precipitate and silicon material in the inserted $SiO_2$ layers during forming process. According to the Poole-Frenkel equation, which is $J \propto E_i \exp\left[\frac{-q\left(\Phi_B - \sqrt{qV/\pi d\varepsilon_i}\right)}{kT}\right]$, we obtain $\ln\left(\frac{J}{V}\right) \propto \ln d - \left(\frac{q\Phi_B}{kT}\right) + \left[\frac{q\left(\sqrt{qV/\pi d\varepsilon_i}\right)}{kT}\right]$. As $\ln d - \left(\frac{q\Phi_B}{kT}\right)$ is constant, by drawing out the curve with axis of $\ln\left(\frac{J}{V}\right)$ and $\sqrt{V}$ we can get

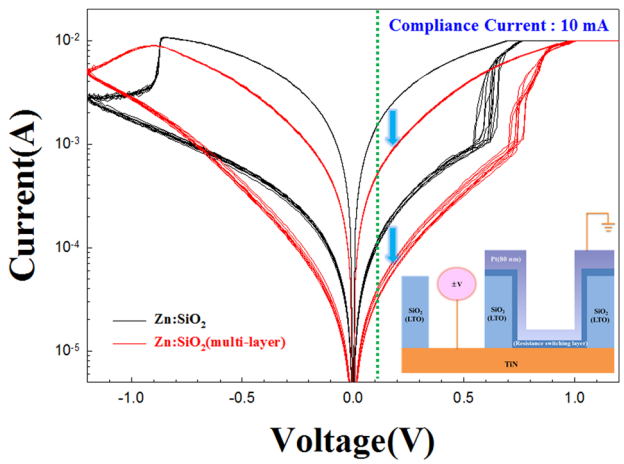


FIG. 5. The bipolar behavior of the RRAM devices using the single Zn:$SiO_2$ layer and multi-layer Zn:$SiO_2$/$SiO_2$ structure. The schematic of RRAM device is shown in the right bottom inset.

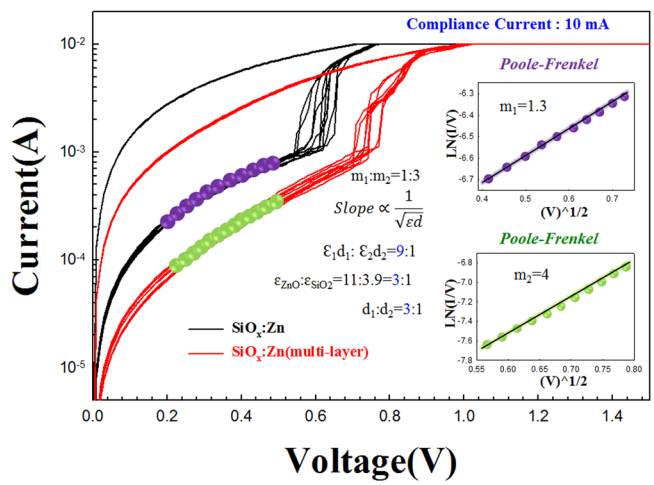


FIG. 6. The HRS current fitting of single Zn:$SiO_2$ layer and multi-layer Zn:$SiO_2$/$SiO_2$ devices. The insets are the corresponding matching degree.

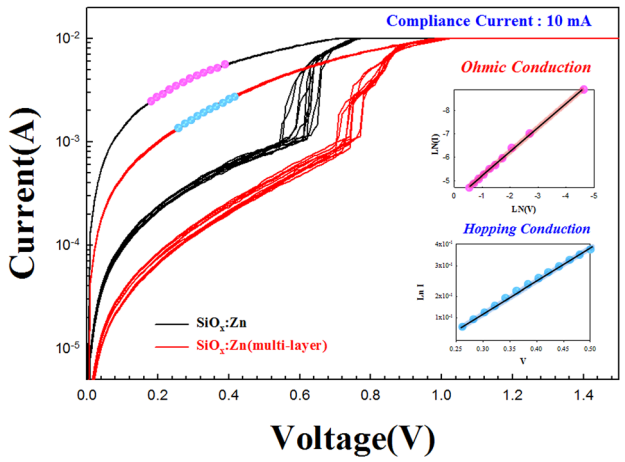


FIG. 7. The LRS current fitting of single Zn:$SiO_2$ layer and multi-layer Zn:$SiO_2$/$SiO_2$ devices. The insets are the corresponding matching degree.

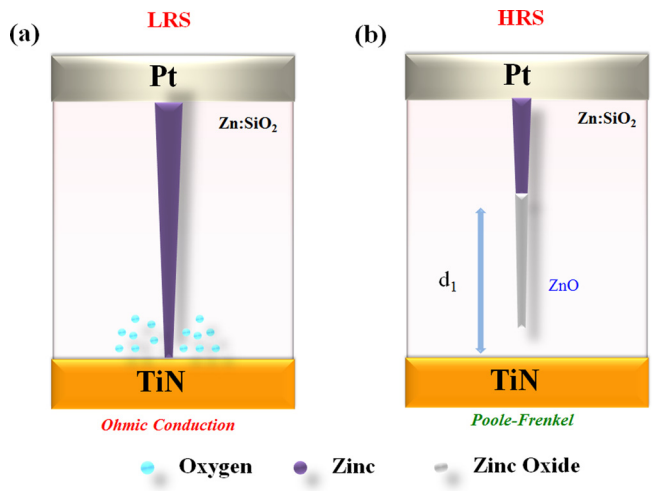


FIG. 9. The schematic diagram of redox reaction in single Zn:$SiO_2$ layer RRAM device.

the fitting curve slope of two devices (insets of Fig. 6). $m_1$ and $m_2$ are the slope of single layer and multilayer device fitting curve, respectively. As $m_1 = 1.3$, $m_2 = 4$, $m \propto \sqrt{\text{const}/d\varepsilon_i}$, and the permittivity ratio between $SiO_2$ and ZnO is $\varepsilon_{ZnO}:\varepsilon_{SiO2} = 11:3.9$,[44,45] we can estimate the ratio of switching layers' thickness between these two devices, which is $d_1:d_2 = 3:1$.

While to the LRS of both devices, it is noted that multilayer device owns hopping conduction, which is quite different from normal Ohmic conduction in single Zn:$SiO_2$ layer device. The common Ohmic conduction ascribes to high concentration metal phase zinc precipitation in Zn:$SiO_2$ thin film, leading to the formation of metal filaments. Together with the XPS analysis of Zn concentration, we think the filament is made of high concentration metal. The carriers conduct through relative complete metal filament, which is in turn registered as Ohmic conduction.[29,38] The Ohmic current conduction mechanism has also been investigated in our previous study.[46] To the multilayer device, the hopping conduction is due to electron carriers surpassing the energy barrier height of each blocking $SiO_2$ layer. By surpassing the spacing $SiO_2$ layer, carriers conduct in a manner of hopping conduction.

In order to further confirm the current conduction mechanism of LRS for these two types of RRAM devices, we measure the I-V characteristics under vary-temperature environment. In Fig. 8, the on state currents of LRS of both types of devices are measured at low temperature with a range from 100 K to 298 K. According to the experimental data, the current of single layer structure RRAM decreases with the rising of the temperature (Fig. 8(a)), which is consistent with Ohmic conduction mechanism property. On contrast, the relationship between conduction current and temperature of multi-layer structure RRAM devices on LRS exhibits the reverse trend (Fig. 8(b)), which complies with hopping conduction equation $J = \alpha n v q \exp(\frac{-U}{kT} + \frac{q\alpha E}{kT})$.

To clarify the conduction mechanism, single layer conduction model and multilayer conduction model are proposed, respectively, as shown in Figs. 9 and 10. In single

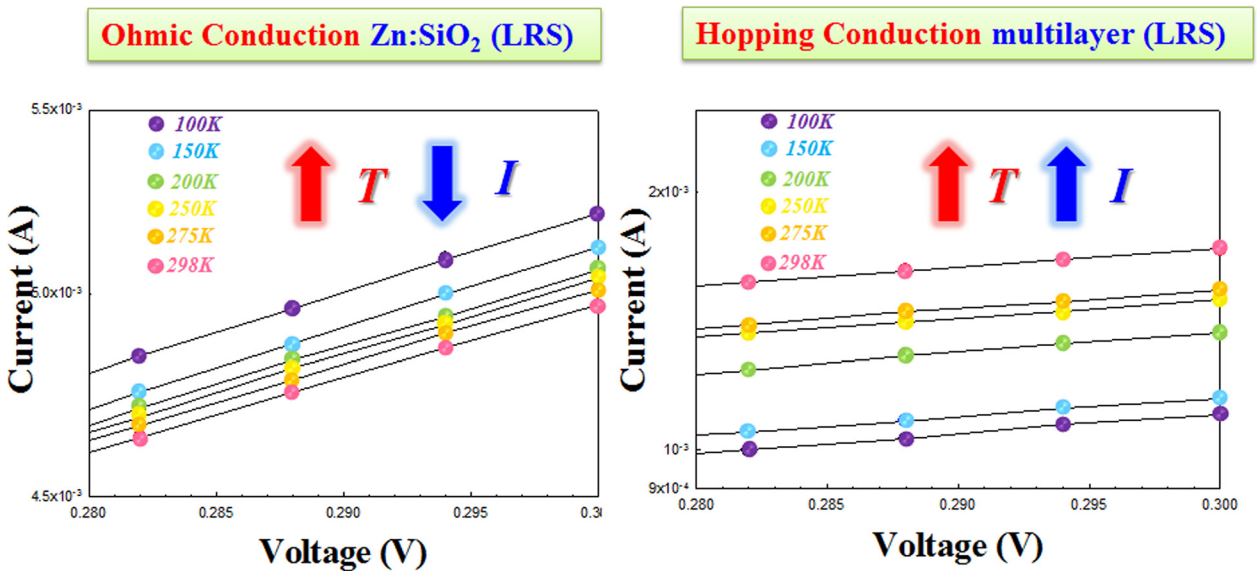


FIG. 8. I-V curves of LRS in single Zn:$SiO_2$ layer and multi-layer Zn:$SiO_2$/$SiO_2$ devices under vary temperature measurement.

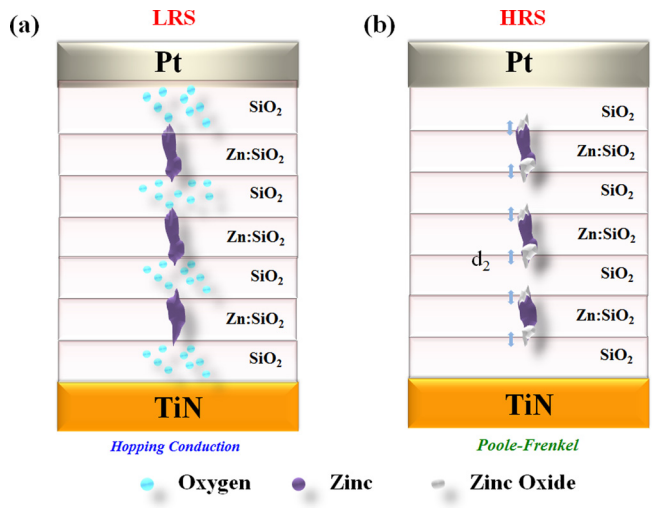


FIG. 10. The schematic diagram of redox reaction in multi-layer $Zn:SiO_2/SiO_2$ RRAM device.

layer device, after electro-forming process, conduction filament is formed. By reducing and oxidizing the tip of metal filament, LRS and HRS can be switched. That is also the reason why LRS exhibits Ohmic conduction mechanism while HRS changes into Poole-Frenkel conduction, as relative complete filament acts as the conduction media in LRS while defects facilitated carrier emission-capture dominates after the filament is oxidized. Compared with single layer RRAM, filament formation process in multilayer devices is restricted with the $Zn:SiO_2$ layers. Owing to the relative incomplete filament in each layer, it is less easily for carriers conduct through, which in turn contributes to the reduction of conduction current density.[37] But there is also an interesting phenomenon, which is the higher operation current for multi-layer RRAM below −0.7 V. This is mainly due to the thinner switching layer, in which the alleviated oxidation effect in reset process happens. Comparatively, drastic oxidation combined with severe thermal effect in the single layer sample dominates, which results in intensely rupture of the filament and thus lower current. Furthermore, we also conducts retention experiments, and the resistance values of LRS and HRS of multilayer $Zn:SiO_2/SiO_2$ RRAM devices can remain almost constant even after $10^4$ s retention performance test at 85 °C, which implies the multilayer device has stable non-volatile memory characteristics.

Normally, when the compliance current is high enough, for example 10 mA, it is not easy to control the over-formation of metal filaments as massive metal ions triggered by electrical and thermal energy migrate to form precipitates. Large quantities of precipitates will lead to the over-formation of metal filaments, which induce current over-shooting phenomenon in the sweeping process. And this phenomenon is even more familiar in metal oxide based RRAM devices due to the high concentration of metal ions.[29,38,46] Thus, with the combination of silicon oxide base and inserting metal-free $SiO_2$ layers into the resistive switching layer, filament formation process is effectively restrained, from which working current reduction and over-shooting elimination can be achieved.

## IV. CONCLUSION

In summary, low electrical power consumption bipolar resistance switching RRAM was fabricated using multilayer stacking technology. By inserting separated metal-free $SiO_2$ layers, over-formation of metal filaments can be avoided, from which we can restrict both the amplitude of operating current and current over-shooting phenomenon. Conduction current fitting was performed to analyze the carrier conduction property and vary temperature experiment was applied to confirm the conduction mechanism. Meanwhile, models for both types of devices were proposed to clarify the resistive switching characteristics. Multi-layer stacking silicon oxide based structure RRAM is a promising candidate for future low electrical power consumption non-volatile memory devices.

## ACKNOWLEDGMENTS

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