JOURNAL OF APPLIED PHYSICS 117, 084502 (2015)

Performance stability and functional reliability in bipolar resistive switching of bilayer ceria based resistive random access memory devices

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(Received 31 October 2014; accepted 12 February 2015; published online 26 February 2015)

Memory devices based on Ti/CeO_{2-x}:CeO_2/ITO stacks with bilayer structure fabricated by rf-magnetron sputtering demonstrate promising bipolar resistive switching behavior with relatively low-voltage operation and small distribution of switching parameters. These devices show much reliable repeatability and good endurance (>10^4 switching cycles) without any significant degradation in their performance. The cycle-to-cycle and device-to-device distribution of resistance switching parameters, such as resistances in the low and high resistance states, set and reset voltages have been investigated and discussed. Resistive switching behavior in our devices has been proposed to originate from the electric field induced drift of defects (specifically oxygen vacancies) preferably along grain boundaries in the bilayer structure of active dielectric layer. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4913504]

I. INTRODUCTION

Resistive switching (RS) is an electric stress (voltage or current) induced reversible and repeatable resistance transformation between two distinct (low and high) resistance states making the device useful for digital memory based read/write applications. Metal-insulator-metal (MIM) structures have attracted considerable interest for their applications in non-volatile memory technology.[1–5] Resistive random access memories (RRAMs) have many advantages over other data storage technologies, such as much faster read/write rate, smaller bit cell size, low operating power, and very large retention times.[2,6–8] Indium tin oxide (ITO) coated glass substrates are widely used in most display applications due to their superior environmental stability, relatively low electrical resistivity, and high transparency.[9,10] Rare-earth metal oxides, such as Yb_2O_3,[11] Gd_2O_3,[12] CeO_2,[13] and Tm_2O_3 (Ref. 14), have shown promising characteristics for applications in non-volatile memory devices because of their high resistivity, large dielectric constant, wide band gap, and good thermodynamic stability.[15] Ceria (CeO_2) is being considered as one of the possible candidates for high-k dielectrics owing to its low leakage tunneling current at low operational voltages,[16,17] low lattice mismatch (0.35%) with silicon,[18] its thermal stability and its ability to grow epitaxially on Si. In addition, ceria has capability to store and release oxygen under oxidizing and reducing conditions, with high surface exchange coefficient for oxygen, which can play vital role in RS memory devices.[19,20] Reports illustrate that resistive switching in ceria based memory devices is associated with formation and rupture of conducting filaments which lead to bipolar and unipolar RS behaviors.[19,21] Simple composition, stable RS behavior, nonstoichiometric distribution of oxygen vacancies, and room temperature deposition make ceria a possible functional material for non-volatile memory applications. In this study, we have investigated the resistive switching properties of room temperature sputtered Ti/CeO_x/ITO memory devices. The observed RS mechanism has been explained on the basis of existing oxygen vacancy model. The low power consumption during SET and RESET transitions as well as good distribution of switching parameters of our device can make it a potential candidate for nonvolatile RRAM applications.

II. EXPERIMENTAL DETAILS

Firstly, an active layer of CeO_2 thin film (~15 nm) was deposited on ITO coated glass substrate at room temperature by radio frequency (RF) magnetron sputtering at RF power of 75 W and pressure of 10 m Torr under Ar-O_2 (10:20) mixture (flow rate = 20 sccm). After deposition, ceria films were annealed at 200 °C for 30 min in oxygen ambient (maintained at 12 mTorr). Then a second ceria layer (having thickness of ~2, 4, 6, 8 nm) was deposited on annealed CeO_2/ITO by RF magnetron sputtering under the same conditions as discussed above to fabricate different structures. Finally, bi-layered top electrode TiN (20 nm)/Ti (50 nm) was deposited on these structures by sequential e-beam evaporation through metal shadow mask (Ø = 150 μm). This yields circular devices with cell size of ~150 μm (in diameter). Here, TiN layer acted as capping layer to avoid the oxidation and scratching of top Ti electrode. The electrical characteristics of TiN/Ti/CeO_{2-x}:CeO_2/ITO devices were examined at room temperature using B1500A semiconductor parameter analyzer. Crystalline structure of the device was determined by X-ray diffraction (XRD) using 3° grazing incidence of Cu K_α (λ = 0.1542 nm) radiations. Film thickness and any interfacial reaction between Ti/CeO_{2-x} were confirmed by cross-sectional high resolution transmission electron microscopy (HRTEM), while elemental composition of the deposited

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layers was determined by energy dispersive X-ray spectroscopy (EDX).

III. RESULTS AND DISCUSSION

XRD pattern of Ti/CeO_{2-x}:CeO_2/ITO stack shown in Fig. 1 depicts weak polycrystalline nature mainly attributable to (111), (200), (220), and (311) orientations in fluorite cubic structure of CeO_2 (ICDD Ref.: 34–0394). As the strongest (111) peak is not much sharp, this behavior may be associated with weak polycrystalline nature and very small thickness of ceria films.[22] XRD reflections related to ITO electrode are also visible in the pattern showing relatively stronger polycrystalline nature. HRTEM micrograph displayed in Fig. 2(a) shows CeO_2 nanograins (inset of Fig. 2(a)) dispersed in a disordered matrix as depicted by XRD pattern. The EDX images of Ti/CeO_{2-x}:CeO_2/ITO device (Fig. 2(b)) show the presence of oxygen (~56%), cerium (~38%), indium (~3%), and titanium (~3%) as determined by energy dispersion at different locations (inset of Fig. 2(a), numbers depict spectrum region). It is believed that an electrically formed oxygen-rich interfacial layer might play key role in improving switching characteristics. That is why a second layer (unannealed) was deposited on annealed CeO_2 layer. The annealed layer is expected to be more stoichiometric than unannealed one because of relatively better crystalline structure and so the second layer is named as CeO_{2-x}. Therefore, relatively large number of defects including oxygen vacancies may be supposed to observe in the CeO_{2-x} layer.

I–V characteristics of Ti/CeO_{2-x}:CeO_2/ITO devices having CeO_{2-x} layer thickness of 2 to 8 nm were studied one-by-one at room temperature. It was noticed that devices with CeO_{2-x} layer thickness of 2 and 4 nm did not show any electroforming and/or any resistive switching behaviour even up to an applied bias of ± 5 V. So these devices were not considered for further studies. However, the structures with 6 and 8 nm CeO_{2-x} layers showed electroforming and resistive switching properties for an applied biasing of ~2 V. The results of various experiments performed on devices with 6 and 8 nm CeO_{2-x} layers indicated that the performance of the device with 6 nm thick CeO_{2-x} layer was much better, reliable, and more stable as compared to that with

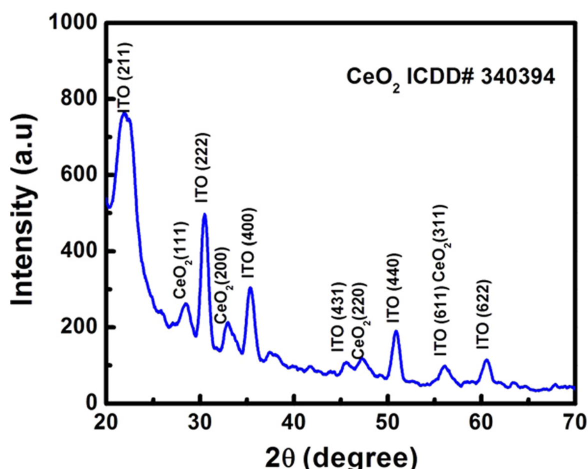

FIG. 1. XRD pattern of Ti/CeO_{2-x}:CeO_2/ITO device.

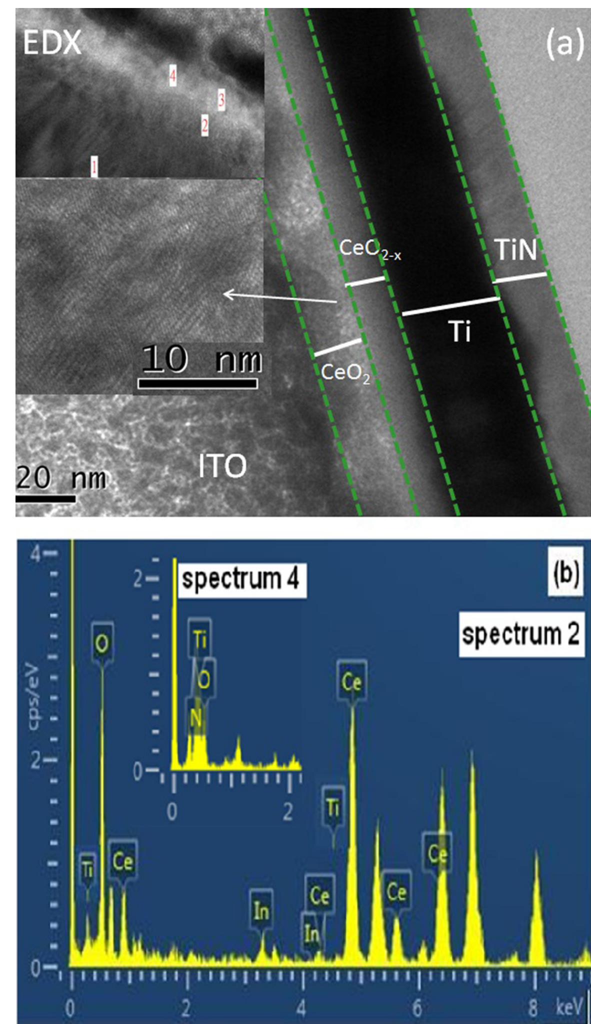

FIG. 2. (a) Cross-sectional HRTEM image, numbers shown in inset image indicate the regions where EDX analyses were performed and (b) EDX images of the Ti/CeO_{2-x}:CeO_2/ITO devices.

8 nm thick CeO_{2-x} layer (results are not shown here), so only the results of the devices with 6 nm thick CeO_{2-x} layer are presented in this research report. The absence of resistive switching in devices with 2 and 4 nm thick CeO_{2-x} layers can be understood as follows: It looks that higher forming voltages (>5 V) and/or higher current compliances (mA) may be needed to activate resistive switching in these devices, which means that higher energy is required to form the conducting filaments. Such behavior might have originated from nano-morphological variations in both ceria layers caused by different oxygen vacancy densities.[23,24] Moreover, bottom ITO electrode is incapable to provide sufficient number of electrons to overcome the traps/defects in the active ceria layers and take part in the conduction mechanism.

It is observed that as-prepared Ti/CeO_{2-x}:CeO_2/ITO devices require electroforming (a positive voltage sweep applied to the top electrode) to trigger resistive switching behavior (at forming voltage of ~2 V and current compliance of 100 μA) as illustrated in Fig. 3(a). The sharp rise in device current (~2 orders of magnitude) in the first voltage sweep analogous to defects-induced dielectric soft breakdown indicates the electroforming caused by breaking of

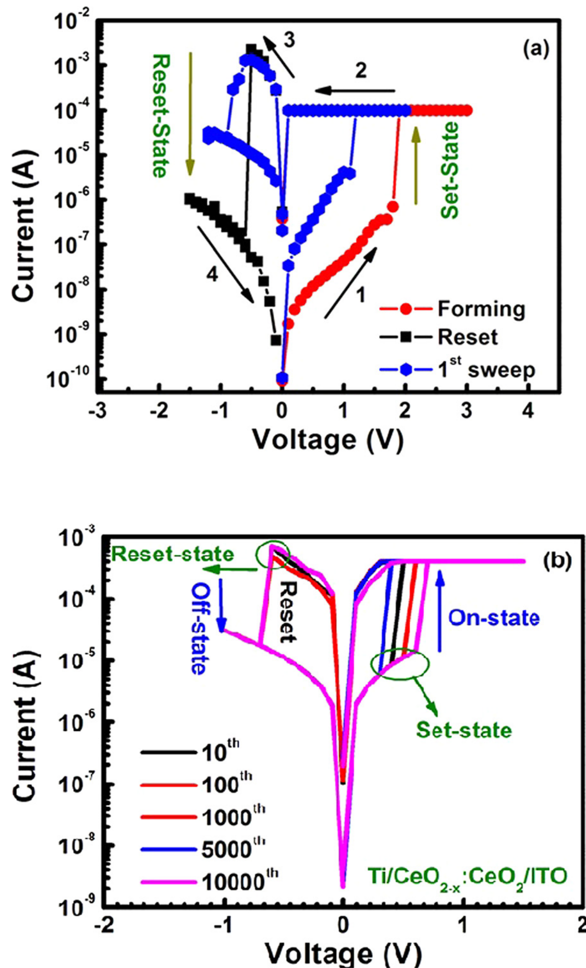

FIG. 3. Analysis of resistive switching characteristics of Ti/CeO_{2-x}:CeO_2/ITO RRAM devices: (a) forming step and the first resistance switching cycle and (b) typical bipolar RS I−V curves after electroforming.

chemical bonds or migration of defects. A large number of defects, such as oxygen vacancies, metallic defects, and dislocations may be generated in active ceria films during forming process, along with oxygen ions migration towards the top Ti electrode. Since Ti is capable of producing oxygen vacancies in the CeO_{2-x} layer due to its oxygen gettering ability.[25] This can further increase the density of oxygen vacancies in the CeO_{2-x} layer as explained earlier. The bilayer structure thus introduces a concentration gradient of oxygen vacancies in the active region. Therefore, switching mechanism of the device can involve the migration of oxygen vacancies under this concentration gradient as a positive bias is applied. The positive bias applied to Ti top electrode repels oxygen vacancies into the CeO_2 layer, which may lead to the formation of conductive paths between the electrodes switching the device into ON-state. Our earlier study reported ITO/CeO_2/ITO devices required electroforming voltages higher than 5 V.[23] But due to the use of Ti top electrode and bilayer structure of the active oxide, a reduction in the forming voltage is noticed. Such low value of electroforming voltage (∼2 V) may be associated with the presence of relatively large number of oxygen vacancies in the CeO_{2-x} layer. On applying negative bias to the top electrode, oxygen vacancies can be attracted back towards the CeO_{2-x} layer. This results in out-diffusion of oxygen vacancies from the conducting paths (filaments), which may lead the device to OFF-state. SET/RESET transitions caused by positive/negative biasing indicate bipolar resistive switching of the device as illustrated in Fig. 3(b). It is also notable that the set and reset voltages in present Ti/CeO_{2-x}:CeO_2/ITO devices are found to be smaller than those of our already reported ITO/CeO_2/ITO [Ref. 23] and Zr/CeO_x/Pt devices [Ref. 19]. Thus, it can be said that the interaction of CeO_2 and CeO_{2-x} layers plays important role in the resistive switching process of Ti/CeO_{2-x}:CeO_2/ITO devices. Moreover, the abrupt RESET transition instead of multistep decreasing current behavior indicates that the underlying mechanism of RESET steps in the present device is analogous to that of ITO/CeO_2/ITO devices reported in Ref. 23 but somewhat different from that of Zr/CeO_x/Pt devices reported in Ref. 19.

The cycle-to-cycle variations of ON- and OFF-state resistances (measured at reading voltage of 0.2 V) for about 11 000 cycles, plotted in Fig. 4(a), show that the device is capable of exhibiting much stable resistive switching persistent with a sufficient memory window in terms of the two well-resolved and stable memory states. The cycle-to-cycle resistances of the most ON-states are in the range of 750–1370 Ω

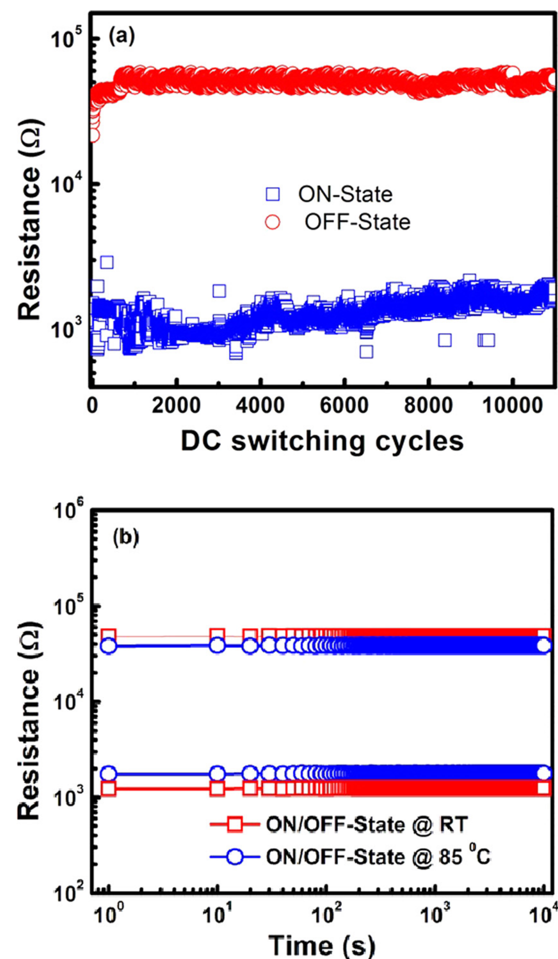

FIG. 4. (a) Endurance characteristics of the Ti/CeO_{2-x}:CeO_2/ITO RRAM devices for continuous voltage sweeping operation illustrating the stability of both HRS and LRS, (b) retention characteristics of both HRS and LRS at RT and at 85 °C.

and resistances of OFF-states lie in the range of $(2.18–4.07) \times 10^4$ Ω. The gradual but small increase in the low resistance state with repeated resistive switching cycles might have originated from the partial dissolution of the stronger conducting filaments due to continuous current flow through them. Whereas the weaker filaments are repeatedly connected and ruptured during successive switching cycling, the stronger filaments conduct current irrespective of whether the device is in low resistance (LRS) or in high resistance state (HRS) (because they are not completely dissolved during RESET process). Continuous current flow through these filaments may cause local Joule heating followed by thermally enhanced migration of the oxygen vacancies from these filaments into those regions where the density of oxygen vacancies is low. Such behavior may be associated with a decrease in conductivity and increase in resistance in the LRS. This small increase in LRS resistance cannot be expected to reflect in HRS which is about two orders of magnitude larger than the LRS and, in contrast to LRS, is not the resistance of the filament. To ensure practical applications of the Ti/CeO_{2-x}:CeO_2/ITO devices, data stress tests were performed at room temperature and at 85 °C under DC stress biasing of ± 0.2 V at an interval of 10 s. As shown in Fig. 4(b), no degradation of resistances in HRS and LRS is noted for more than 10^4 s. Such good endurance and retention properties provide a perspective that the Ti/CeO_{2-x}:CeO_2/ITO memory devices have potentials as suitable candidates for non-volatile memory applications.

Fig. 5 depicts the statistical distributions of V_{set} and V_{reset} for cycle-to-cycle (C2C) and device-to-device (D2D) testing in dc sweeping mode. It is noted that for a single device, the distribution is not much wider (Fig. 5(a)) making the device suitable for memory applications. However, when test was performed on so many devices, slightly wider range of V_{set} and V_{reset} distribution in D2D analyses (Fig. 5(b)) was found which may be attributed to non-uniform distribution of oxygen vacancies in the CeO_{2-x} layer in different devices.[26] In connection with the conducting filament model,[27] the C2C and D2D dispersion in switching parameters can be reduced by controlling the filament formation and rupture, which usually takes place at top electrode and metal oxide interface. Since Ti is more capable to attract oxygen ions than ITO, it is expected that the CeO_2-ITO interface might be sharp and well-defined as compared to the Ti-CeO_{2-x} interface which is rather blunt because of the diffusion of oxygen ions from CeO_{2-x} layer towards Ti through it. However, the CeO_{2-x}-CeO_2 interface is the one across which maximum diffusion of oxygen vacancies takes place.

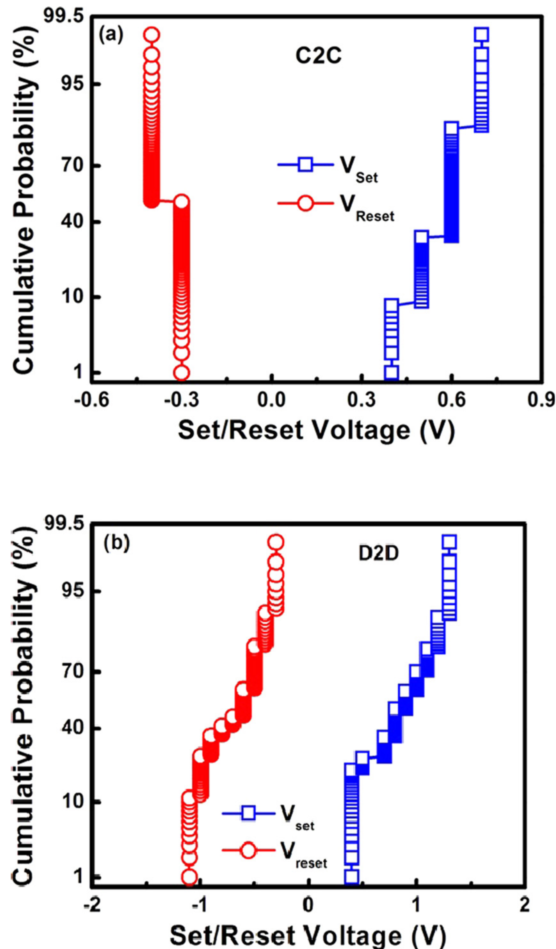

FIG. 5. Cumulative probability distributions of V_{set} and V_{reset} voltages for (a) C2C and (b) D2D measurements.

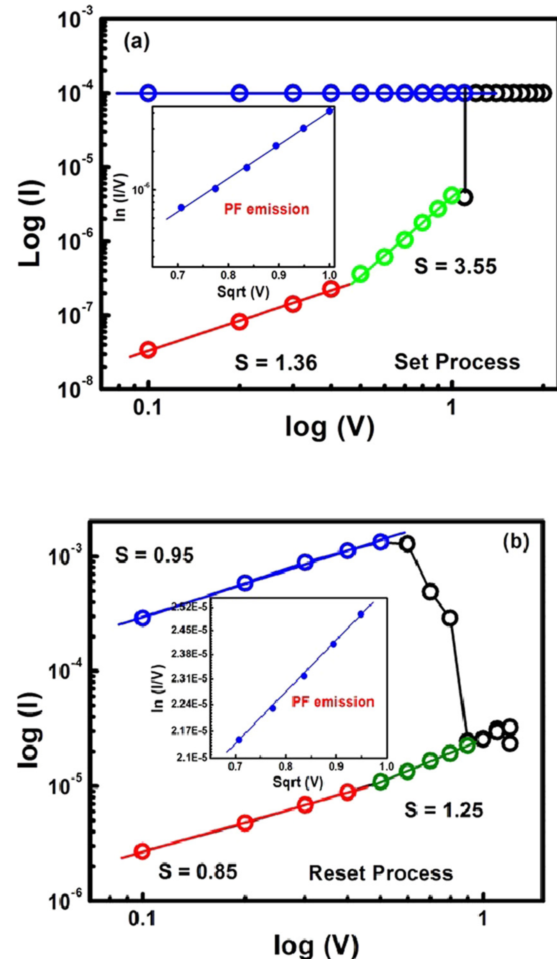

FIG. 6. The log (I)-log (V) plots of the Ti/CeO_{2-x}:CeO_2/ITO memory devices. The insets depict fitting plots for Poole-Frenkel conduction at high voltage region in the HRS.

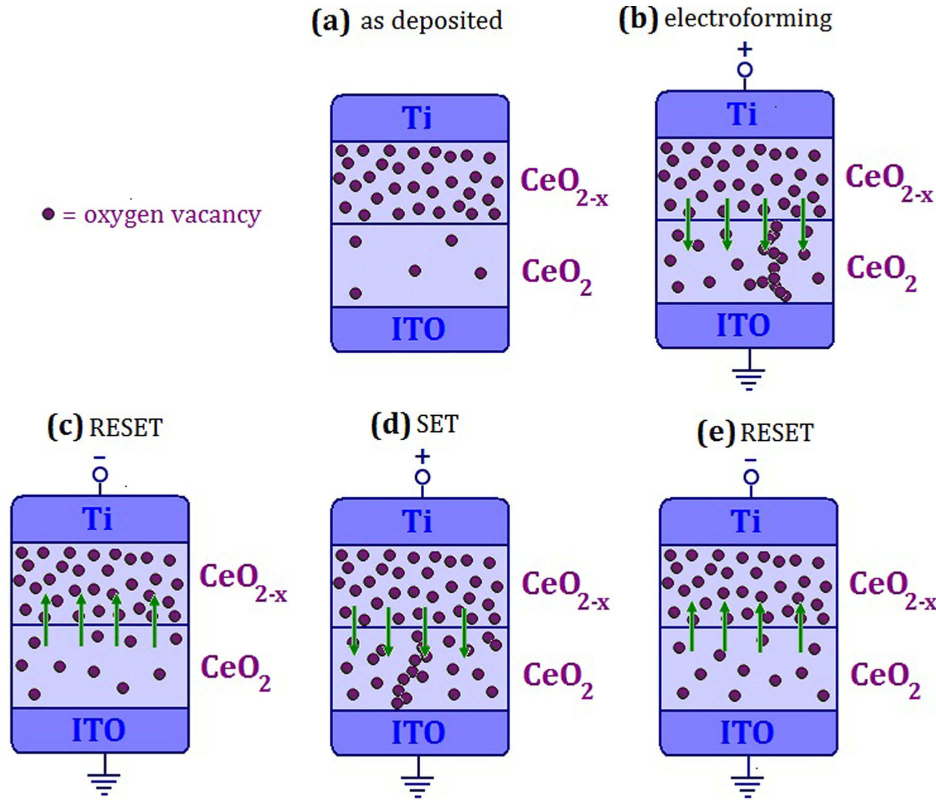

FIG. 7. Schematic illustration of (a) pristine state, (b) forming mechanism, (c) RESET process, (d) SET process, and (e) RESET process in Ti/CeO_{2-x}:CeO_2/ITO devices.

It may be oxygen-vacancy-rich in SET state and oxygen-vacancy-deficit in RESET state.

LogI-logV plots in the LRS are completely linear (slope ∼0.95) as illustrated in Fig. 6 and the mechanism behind such slope can be explained as the formation and rupture of localized conducting filaments leading to Ohmic transport of carriers. I–V characteristics plotted in Fig. 6 demonstrate that Ohmic conduction also prevails in the low voltage regime in HRS of both ON- (slope ∼1.36) and OFF-states (slope ∼0.85). However, in high voltage regime, slope of these I–V plots changes to 3.35 in the ON-state (Fig. 6(a)) and 1.25 in the OFF-state (Fig. 6(b)), which rules out the possibility of space-charge conduction (Child's Law: $I \propto V^2$). Moreover, linear plots between ln (I/V) and $V^{1/2}$ shown in the insets of Figs. 6(a) and 6(b) reveal Poole-Frenkel (PF) type conduction mechanism to be operative in high field regions. In PF-conduction, applied field induced lowering of Coulomb potential barrier at trapping sites allows the trapped carriers to deplete these sites and involve in the conduction process.[28–31] Most likely, the defects related to structural disorder and non-stoichiometry in the ceria layer act as trapping sites for the charge carriers. Under these conditions, the bulk-limited PF-conduction at high applied electric field is quite probable.

It is quite rational to assume that oxygen vacancies play vital role in the resistive switching behavior of ceria layers.[32] Here, Ti metal works as oxide dissociation catalyst which might affect kinetics of the interface reaction by creating oxygen vacancies in the CeO_{2-x} layer and producing a concentration gradient (Fig. 7(a)) as discussed earlier. By applying positive biasing, these oxygen vacancies arrange themselves to form localized conducting filaments as shown in Fig. 7(b) (electroforming). During successive negative voltage sweep, filaments near the CeO_{2-x}:CeO_2 interface can be more easily oxidized and ruptured (RESET process) due to migration of oxygen vacancies/ions across the interface (Fig. 7(c)).[33,34] In the subsequent SET step (Fig. 7(d)), the positive voltage applied to the top electrode pushes oxygen vacancies from the bulk of top CeO_{2-x} layer back into the lower CeO_2 layer. These oxygen vacancies preferably drift along grain boundaries, and rearrange to repair the ruptured filaments. The conductive filamentary paths are continuous but cannot necessarily be straight (because the oxygen vacancies have to arrange themselves along grain boundaries). The later

TABLE I. Comparison of operational characteristics with other rare-earth oxides based RRAM devices.

Stability test	GdO_x (Ref. 35)	Eu_2O_3 (Ref. 36)	Lu_2O_3 (Ref. 37)	Sm_2O_3 (Ref. 38)	CeO_2 (This work)
V_{set}/V_{reset} (V)	+3/−3	+5.2/−7.2	+1.2/−0.8	+1.0/−0.3	+0.6/−0.3
Current compliance (μA)	300	10	100	100	100
Endurance (cycles)	10^4	300	800	10^4	10^4
Resistance ratio	100	2.89×10^3	10^4	100	40
Retention time (s)	10^4	10^4	10^3	10^5	$>10^4$

RESET process induced by negative bias is also illustrated in Fig. 7(e).

A comparison of operational parameters concerning resistive switching behavior for different rare-earth oxides (REOs) based RRAM devices has been made in Table I. It is notable that ceria is among the REOs with relatively better resistive switching characteristics. Moreover, as far as power consumption is concerned, our ceria based memory devices possess better operational characteristics (lower values of V_{set} and V_{reset}) as compared to other RRAM devices. The each listed RRAM device has different active oxide thicknesses. However, the range of thickness is not too wide to compare these devices.

IV. CONCLUSIONS

In summary, a stable, reproducible, and reliable bipolar resistive switching has been studied in room temperature sputtered Ti/CeO_{2-x}:CeO_2/ITO devices for more than 10 000 cycles. In LRS, current conducts through Ohmic mechanism. However, in HRS, conduction is Ohmic at low applied fields only but of Poole-Frenkel nature at high fields. While switching mechanism is found to be governed by the migration of oxygen vacancies/ions across the CeO_{2-x}:CeO_2 interface. Cycle-to-cycle performance uniformity as well as device-to-device uniformity in switching parameters has also been reported. The device demonstrates sufficiently long data retention over 10^4 s both at room temperature and at 85 °C. These good resistive switching characteristics of Ti/CeO_{2-x}:CeO_2/ITO devices show their potential in the field of non-volatile RS memory applications.

ACKNOWLEDGMENTS

This work is supported by Higher Education Commission (HEC), Islamabad Pakistan. Authors are also grateful to Professor Dr. T. Y. Tseng, Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan for providing experimental facilities and useful suggestions.

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