Perpendicular spin transfer torque magnetic random access memories with high spin torque efficiency and thermal stability for embedded applications (invited)

Luc Thomas,[a] Guenole Jan, Jian Zhu, Huanlong Liu, Yuan-Jen Lee, Son Le, Ru-Ying Tong, Keyu Pi, Yu-Jen Wang, Dongna Shen, Renren He, Jesmin Haq, Jeffrey Teng, Vinh Lam, Kenlin Huang, Tom Zhong, Terry Torng, and Po-Kang Wang
TDK-Headway Technologies, Inc., Milpitas, California 95035, USA

(Presented 5 November 2013; received 24 September 2013; accepted 15 October 2013; published online 15 April 2014)

Magnetic random access memories based on the spin transfer torque phenomenon (STT-MRAMs) have become one of the leading candidates for next generation memory applications. Among the many attractive features of this technology are its potential for high speed and endurance, read signal margin, low power consumption, scalability, and non-volatility. In this paper, we discuss our recent results on perpendicular STT-MRAM stack designs that show STT efficiency higher than $5\,k_BT/\mu A$, energy barriers higher than $100\,k_BT$ at room temperature for sub-40 nm diameter devices, and tunnel magnetoresistance higher than 150%. We use both single device data and results from 8 Mb array to demonstrate data retention sufficient for automotive applications. Moreover, we also demonstrate for the first time thermal stability up to 400 °C exceeding the requirement of Si CMOS back-end processing, thus opening the realm of non-volatile embedded memory to STT-MRAM technology. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4870917]

Since first introduced in the mid 1990s, magnetic random access memories (MRAMs) have generated much interest because of their inherent non-volatility, high write speed, and potentially infinite endurance.[1,2]

MRAM cells are based on magnetic tunnel junctions (MTJs) comprising two ferromagnetic electrodes separated by a thin tunnel barrier. Owing to the tunnel magnetoresistance (TMR) phenomenon,[3] parallel and antiparallel alignment of the ferromagnetic electrodes of the MTJs give rise to low or high resistance states corresponding to 0 or 1 logic states, respectively (Fig. 1(a)). The read signal, hence the speed at which the bits can be read, depends on the TMR ratio. While the TMR ratio was limited to about 70% at room temperature in earlier MTJs based on amorphous Aluminum oxide barriers, tremendous improvement has followed the 2004 discovery of TMR through crystalline MgO tunnel barrier.[4,5] Values exceeding 600% at room temperature have been reported in 2008 by Ikeda and coworkers.[6]

First generation MRAM cells were built using MTJs magnetized in the plane of the constituting layers and written using localized magnetic fields created by an array of metallic lines. This raised multiple technical challenges, most of which could be overcome by material engineering and cell design improvements.[7–9] However, even though chips are actually commercialized, the market for these chips has remained fairly small due to the high power consumption and limited scaling potential inherent to the use of magnetic fields.

The demonstration that MRAM cells could be written by spin transfer torque (STT) from spin-polarized electrical current[10,11] instead of a magnetic field rekindled the interest in MRAM technology.[12–15] Indeed, contrary to Field MRAMs, the same bit lines can be used to read and write STT-MRAM cells by simply driving current directly through the cell (Fig. 1(b)). This allows for much simpler design,

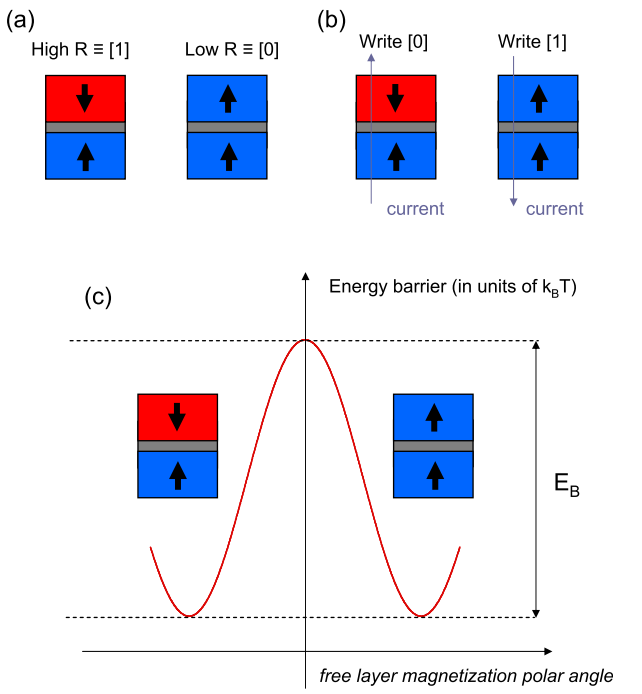

FIG. 1. (a) Schematic of a PMA-MTJ STT-MRAM cell, indicating the logic states of the device with the corresponding resistance levels. (b) Memory cells are written by switching the magnetization of the free layer (top) using STT from spin polarized current. [0] or [1] logic states can be written by simply reversing the current polarity. (c) Perpendicular magnetic anisotropy creates the energy barrier between the two orientations of the free layer's magnetization.

[a]Author to whom correspondence should be addressed. Electronic mail: luc.thomas@headway.com.

denser layout, improved scalability, and power consumption. The latest development of in-plane STT-MRAMs was reported recently by Everspin Technologies, which has demonstrated a fully functional 64 Mb STT-MRAM chip.[16]

Nevertheless, in-plane STT-MRAMs face significant challenges. First, as the cell size is scaled down to 50 nm and below, it becomes increasingly difficult to maintain non-volatility using conventional magnetic materials magnetized in the plane of the MTJ. Non-volatility requires the orientation of the magnetic electrodes to be stable against thermal fluctuations. Thermal stability is determined by the energy barrier E_B separating the two stable orientations of the magnetization of the free layer of the MTJ (Fig. 1(c)). Although the requirement depends significantly on chip design and applications, values larger than 55 k_BT ($k_B = 1.38\,e^{-16}$ erg/K is the Boltzmann constant and T = 300 K at room temperature) are needed to guarantee data retention for 10 yr.[17,18] E_B is the product of the magnetic anisotropy of the free layer and an activation volume which depends on the size of the MTJ. For in-plane magnetized materials, the anisotropy relies almost completely on the weak shape anisotropy of the needle-shaped MTJ cell. Significant energy barriers can only be achieved for large cells. Moreover, controlling the shape of the cell, which is crucial to avoid wide distributions of energy barrier, might prove increasingly difficult as the technology node shrinks down to 22 nm and below. The second challenge is that STT switching of in-plane devices is relatively inefficient because of the out-of-plane precession of the magnetization during reversal, which contributes to the switching current I_{c0} but not to the energy barrier.[19] The STT efficiency, defined by the ratio of the thermal stability factor $\Delta = E_B/k_BT$ and I_{c0}, is typically of the order of 0.1 $k_BT/\mu A$ for in-plane devices.

These limitations can be alleviated by using materials magnetized perpendicular to the plane of the wafer.[20] Indeed, the perpendicular magnetic anisotropy (PMA) that arises, for example, at the interface between MgO and CoFeB[21,22] is strong enough to enable scaling down to sub-20 nm devices.[23,24] Moreover, STT efficiency is more than order of magnitude larger than that of in-plane devices.[24,25]

In this paper, we discuss the development of PMA-MTJ stacks that combine the highest STT efficiency reported to date with extremely high energy barriers and high TMR ratios. We use both single device data and results from 8 Mb MTJ array to demonstrate that our PMA-MTJ stack is capable of providing data retention sufficient for memory operation in high-stress environments such as automotive applications. Moreover, we show that our stack is stable at 400 °C for more than 90 min, thus meeting the requirements of embedded memory applications.

The data discussed in this paper have been collected on devices fabricated at TDK-Headway using conventional UV-photolithography on 8 in. wafers. The PMA-MTJ stacks are deposited using a Canon-Anelva 7100 deposition system and processed in our backend semiconductor facility. We discuss two types of experiments performed on either individual MTJ devices or 8 Mb STT-MRAMs chips. The 8 Mb chips consist of an array of MTJs integrated on 90 nm CMOS technology (Fig. 2(a)). The chip uses a 1 Transistor/1 MTJ memory cell architecture[8,26] with a cell size of $50F^2$.

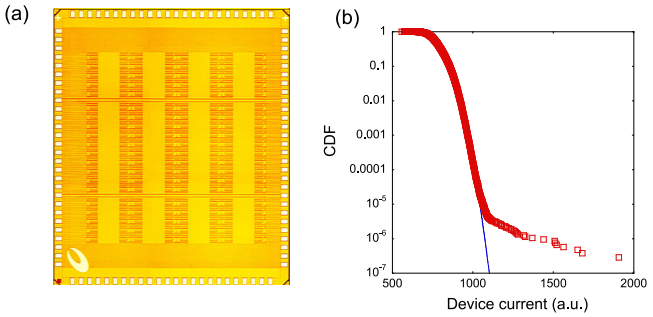

FIG. 2. (a) Optical microscopy image of the 8 Mb memory chip. The chip area is 5.1 × 4.36 mm^2. (b) CDF of the device signal measured for the entire 8 Mb chip. The solid blue line shows the fit of the distribution to an error function. Deviations from the fit at high device current indicate defects (partial shorts). There are less than 10 ppm defects in the chip.

We have recently reported successful writing, data retention, and endurance on those chips.[27]

By optimizing both the MTJ stack and the device integration process, we have been able to achieve extremely low defect rates. The cumulative distribution function (CDF) of the bit signal measured on a typical 8 Mb chip is shown in Fig. 2(b). Data shown here are raw data measured on the entire chip. Defects corresponding to partially shorted bits are apparent in the tail of the distribution. In this example, there are fewer than 10 parts per million (ppm) defects. This level of defect is small enough to be readily repaired by using redundancy.

A PMA-MTJ stack suitable for STT-MRAM applications must be capable of providing the read and write margins, endurance, power consumption, data retention, scaling, and switching performance compatible with the target memory market. This means that the MTJ stack must meet not only one or a few but all the required criteria in terms of TMR, device resistance, STT efficiency, energy barrier, perpendicular anisotropy, offset field, dielectric breakdown, defect rate, etc. Optimizing these different properties may require following very different and sometimes even opposite routes. For example, very strong interfacial PMA is observed in multilayers having f.c.c. crystal structures textured in the (111) direction,[28] whereas high TMR using MgO tunnel barrier requires a b.c.c crystal structure with a (001) texture.[29]

Besides, there are other important, albeit often overlooked constraints associated with specific memory markets. Advanced backend of line (BEOL) processing of CMOS chips requires deposition of the low-k dielectric at 400 °C. Any technology suitable for embedded memory applications must be compatible with this back-end process. Thus, in order for STT-MRAM technology to penetrate this huge and rapidly growing market,[30] the PMA-MTJ stack must withstand 400 °C for an extended period of time. The main challenge here is not the MTJ itself: pseudo spin-valves comprised Ta/CoFeB/MgO/CoFeB/Ta have been shown to withstand anneal temperatures up to 525 °C, provided the CoFeB layers are thick enough (more than 4 nm) to prevent Ta diffusion to the MgO barrier.[6] However, the interfacial PMA in such thick CoFeB layers is too weak to overcome the shape anisotropy, and this structure cannot be used for PMA-MTJs. Indeed, the most significant challenge is designing magnetic electrodes whose

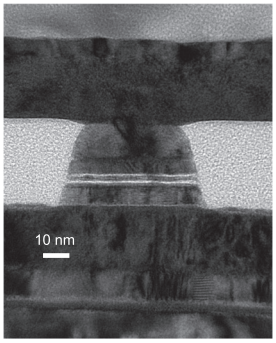

FIG. 3. Cross-sectional transmission electron microscopy image of a fully functional device integrated on 90 nm CMOS. The diameter of this device is about 50 nm.

PMA is not affected by 400 °C BEOL anneal, while avoiding any element detrimental to MTJ properties that can easily diffuse at moderate temperatures, such as Mn,[31] Pd, or Pt.

The results discussed in this paper have been obtained using PMA-MTJ stacks based on a CoFeB free layer sandwiched between two MgO tunnel barriers.[25] A transmission electron microscopy (TEM) image of a typical device is shown in Fig. 3. Since the MgO/CoFeB interface is the source of PMA in this structure,[21,22] the PMA is significantly enhanced by using two such interfaces compared to, e.g., MgO/CoFeB/Ta free layer. Moreover, using a dual MTJ structure prevents the formation of the magnetic dead layer which results from atomic intermixing at the CoFeB/Ta interface.[21] The main challenge of dual MgO barriers is achieving high TMR while maintaining sufficiently low resistance area (RA) product. By adjusting the oxidation conditions, we have obtained TMR ratios higher than 150% for PMA-MTJ stacks with RA $\sim 12\ \Omega\ \mu m^2$.

Fig. 4(a) shows the evolution of the TMR of a PMA-MTJ stack as a function of the anneal time at 400 °C. The data points in the figure show median values of more than 140 devices having diameters between 70 and 90 nm. The TMR increases rapidly up to 100% in the first 10 min of anneal. This behavior has been reported in the literature and is attributed to the crystallization of the amorphous CoFeB layer templated by the MgO barrier.[32,33] Most remarkably, for longer anneal times up to at least 90 min, the TMR is mostly unchanged. It even increases slightly from 130% up to 136% between 30 and 90 min. These conditions far surpass the thermal budget required for embedded memory applications.

As mentioned above, the high thermal stability of our PMA-MTJ is a consequence of the thermal stability of the magnetic electrodes. This is illustrated in Fig. 4(b), which shows examples of resistance vs magnetic field (RH) loops measured on the same device after 30, 60, and 90 min anneal at 400 °C. The squareness of the hysteresis loops shows that the pinned layer remains highly stable in the presence of magnetic fields up to at least 4 kOe. Moreover, the switching field of the free layer is almost unchanged upon annealing, indicating that the anisotropy does not decrease during anneal. This device exhibits a TMR of 153% after 90 min anneal. Most importantly, the offset field arising from the dipolar field of the reference layer is less than 100 Oe, much smaller than the coercive field of more than 3 kOe.

The properties of two representative PMA-MTJ devices are shown in Figs. 5 and 6. These devices are fabricated from two different MTJ stacks labeled A and B hereafter. Stack A is optimized for high STT efficiency while stack B is optimized toward high energy barriers. Both devices have an estimated diameter of 27 nm. Note that diameters reported in this paper are electrical diameters calculated from the resistance of the devices by using local RA values measured on large structures (150–300 nm diameter). Figs. 5(a) and 5(b) show RH and resistance vs. voltage hysteresis loops, respectively, for the device made from stack A. Figs. 6(a) and 6(c) show the switching probability P_{SW} as a function of the applied field for the devices made of stacks A and B, respectively. Figs. 6(b) and 6(d) show 1-P_{SW} as a function of the applied current with no external field.

The field dependence of P_{SW} is well fitted using a simple thermal activation model, allowing us to estimate the anisotropy field H_K and the thermal stability factor Δ. Instead of the commonly used Sharrock model,[34] which applies only to relaxation measurements at constant field, we use a model valid for fixed field sweep rate R[35]

$$P_{SW}(H) = 1 - \exp\left[\frac{-H_K f_0 \frac{\sqrt{\pi}}{2}}{R\sqrt{\Delta}} erfc\left[\sqrt{(\Delta)}(1 - H/H_K)\right]\right], \quad (1)$$

where $f_0 \sim 1$ GHz is the attempt frequency and erfc is the complementary error function. Note that the parameter H_K in

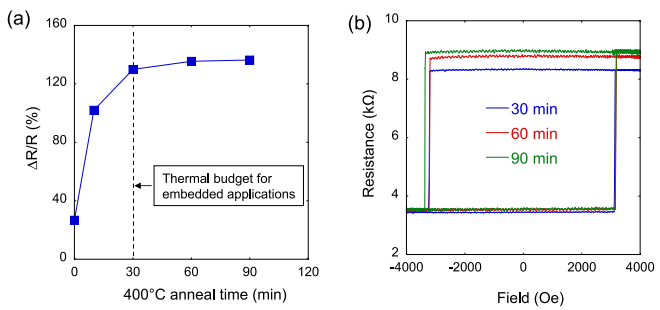

FIG. 4. (a) TMR ratio as a function of anneal time at 400 °C. Data points show the median value of more than 140 devices with a median diameter of 80 nm. (b) Resistance vs. field hysteresis loops of a typical device measured after different anneal times.

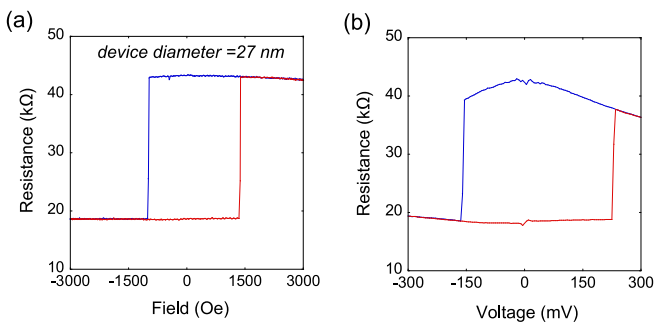

FIG. 5. Device resistance as a function of magnetic field (a) and applied voltage (b) for a device made from MTJ stack A.

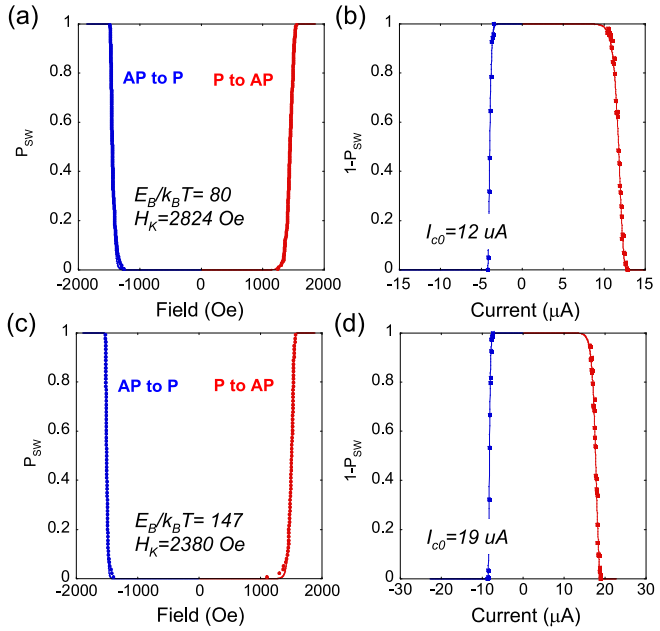

FIG. 6. Switching probability P_{SW} as a function of magnetic field (a) and (c) and current (b) and (d). Top and bottom panels show results for two devices made from MTJ stacks A and B, respectively. Both devices have a diameter of 27 nm. Solid symbols and solid lines show data points and fits to Eqs. (1) and (2), respectively. Parameters extracted from the fits are indicated on the figures. The field dependence of P_{SW} is determined by measuring the distribution of switching fields for both P to AP and AP to P switching on many RH loops (typically more than 150). The field sweep rate is fixed at R = 40 kOe/s and the read voltage is 10 mV. The current dependence of P_{SW} is obtained by probing the resistance state after up to 200 current pulses of length t_p = 1 ms.

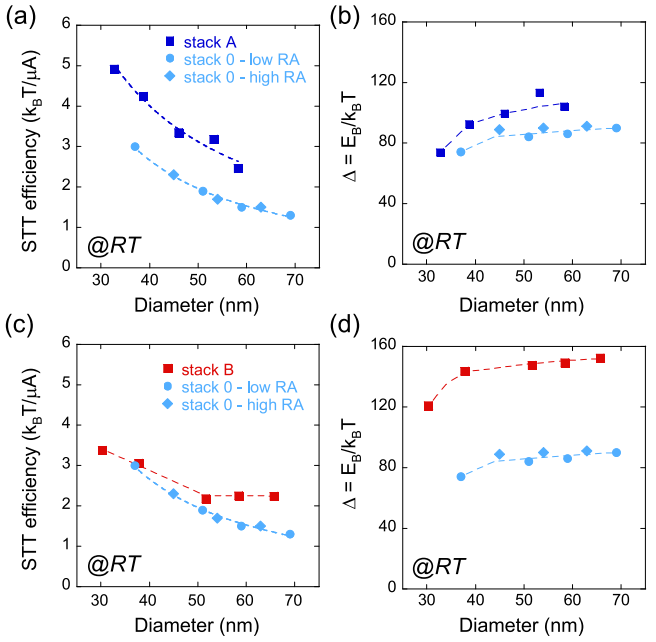

FIG. 7. Spin transfer torque efficiency Δ/I_{c0} and thermal stability factor Δ as a function of device diameter for MTJ stacks A and B. Previous results published in Ref. 25 are also shown for comparison. These data had been obtained from two similar stacks (stack 0) having resistance-area products RA of 6.6 and 12.1 $\Omega.\mu m^2$, respectively. Data point shows median values of up to 100 similar devices. Dashed lines are guide to the eye. All data have been taken at room temperature.

this expression is the field at which the energy barrier vanishes. It is only equal to the anisotropy field for coherent magnetization reversal when the external field is applied along the easy axis. For simplicity, we refer to this field as the anisotropy H_K in the following.

The critical switching current I_{c0} is obtained by fitting the current dependence of P_{SW} to in the thermally assisted STT regime[36]

$$P_{SW}(I) = 1 - \exp\left[-f_0 t_p \exp(-\Delta(1 - I/I_{c0}))\right]. \quad (2)$$

Several groups have recently reported theoretical studies of the relaxation rate in the thermally assisted STT regime in the case of uniaxial—rather than easy plane—anisotropy, which is relevant to PMA-MTJs.[37–39] All these studies find a quadratic current dependence of the relaxation in the form $(1 - I_c/I_{c0})^2$. We find that the values of I_{c0} derived using this quadratic form are about 25% larger than those obtained using Eq. (2). For consistency with previous reports,[24,25] we use Eq. (2) in order to estimate I_{c0}. The value of the STT efficiency Δ/I_{c0} derived from these fits for the two devices shown in Figs. 6(a) and 6(b) and Figs. 6(c) and 6(d) are 6.7 and 7.7 $k_BT/\mu A$, respectively.

We have measured devices of nominal diameters between about 30 to 70 nm. Many different devices (up to 100) have been measured for each size. Fig. 7 shows the median value of Δ/I_{c0} and Δ at each diameter derived using the fitting procedure described above for devices made from stacks A and B. Our previous results published in Ref. 25, labeled stack 0, are also shown for comparison. For both stacks A and B, the STT efficiency increases for smaller devices, in agreement with our previous results (Figs. 7(a) and 7(c)). This dependence follows from the fact that I_{c0} scales with the device area (that is, the critical current density J_{c0} is independent of device area), whereas Δ depends only weakly on the device size (see Figs. 7(b) and 7(d)). This weak dependence of Δ on device area is attributed to the non-uniform nature of magnetization reversal in this range of diameters.[40,41] By contrast, Δ is expected to scale linearly with device area for devices smaller than ~30 nm, in which the magnetization reverses by coherent rotation.

Both stacks A and B show significant improvements compared to our previous results. Indeed, both stacks combine high STT efficiencies with excellent thermal stability. In the case of stack A, 30-nm diameter devices have STT efficiencies of 5.0 $k_BT/\mu A$ and energy barriers of 75 k_BT. Similar devices made from stack B have STT efficiencies of about 3.3 $k_BT/\mu A$—comparable to our previous result[25]—but their energy barriers far exceed 100 k_BT. The fact that small devices exhibit such high barriers illustrates the benefits of using PMA rather than in-plane MTJs. Data reported by Everspin Technologies in Ref. 16 on in-plane STT-MRAMs show that energy barriers of 100 k_BT are only achieved for device area of about 0.013 μm^2, more than 10 times larger than our PMA-MTJ devices.

The high energy barriers measured on sub-40 nm single devices, combined with the thermal stability of our MTJ stack at 400 °C, can open whole new markets to STT-MRAMs. For example, automotive applications require data retention for 10 years at 150 °C. In order to quantify the value of the energy

barrier needed to comply with this requirement, let us assume that there should less than 1 error per million bits for 10 yr at 150 °C. This corresponds to an energy barrier of about 78 kBT at room temperature. However, when device to device distributions are taken into account, higher values are needed. For example, assuming a Gaussian distribution of energy barriers with a coefficient of variations CV = 5% (CV is the ratio of the standard deviation to the mean value), the requirement at room temperature becomes 85 k_BT. If CV reaches 8%, the requirement exceeds 100 k_BT. Furthermore, one must also account for the temperature dependence of the anisotropy field H_K, which is likely to reduce the energy barrier even further above room temperature.

In order to corroborate the results obtained on single devices, we have performed time dependent coercivity measurements on 1 Mb subsets of the 8 Mb array. In these experiments, we measure the fraction of switched devices as a function of dwell time t_w at constant applied field.[25] This allows us to extract the time dependent coercive field $H_C(t_w)$ which is fitted to the Sharrock formula[34] in order to extract Δ and H_K

$$H_C(t_W) = H_K\left(1 - \sqrt{\ln(f_0 t_W/\ln 2)/\Delta}\right). \quad (3)$$

Results are shown in Fig. 8 for 45-nm diameter devices fabricated from two different MTJ stacks. The first stack is similar to that used for our previously published data (stack 0). The second stack is similar to stack B, which gives rise to the highest energy barriers in single device measurements. For both MTJ stacks, Δ and H_K are varied across the wafer by adjusting the deposition conditions. Note that these experiments were performed at 90 °C.

Figs. 8(a) and 8(b) show H_C as a function of $\ln(t_W)$ for stacks 0 and B, respectively. Different symbols correspond to different positions across the wafers. The thickness of some of the layers in the stack is changed across the wafer in order to adjust the value of H_K. Solid lines show fits to Eq. (3). The values of H_K and Δ extracted from these fits are shown in Figs. 8(c) and 8(d), respectively. Interestingly, while stack 0 and stack B give rise to similar values of H_K, they have very different values of Δ. In the case stack 0, the increase of H_K across the wafer is associated with a decrease of Δ, whereas Δ increases across the wafer for stack B. The maximum value observed is Δ = 98 at 90 °C.

We have performed data retention measurements using MTJ stack B as a function of the baking time at elevated temperatures. For this experiment, two 10 kb subsets of the memory array were first reset in the P and AP states, respectively, and the number of bits flipped was recorded as a function of the baking time. Median device diameter is about 48 nm for this set of data. Since no error was observed after more than a week at 150 °C, the data retention test was performed again at 230 °C for up to 2 weeks so as to enhance the failure rate. Results are shown in Fig. 9. Since the stray field from the pinned layer is not perfectly compensated in this stack, the failure rate is slightly higher for AP to P (Fig. 9(a)) compared to P to AP (Fig. 9(b)) switching. As shown in Figs. 9(a) and 9(b), data retention varies significantly depending on the position on the wafer. These variations are consistent with the variations of the energy barrier measured at 90 °C. At the location corresponding to the highest energy barrier (position 8), only 2 and 5 errors are observed after 2 weeks at 230 °C for P to AP and AP 2 P switching, respectively.

From these data retention experiments, we can estimate the median energy barrier at 230 °C as a function of the

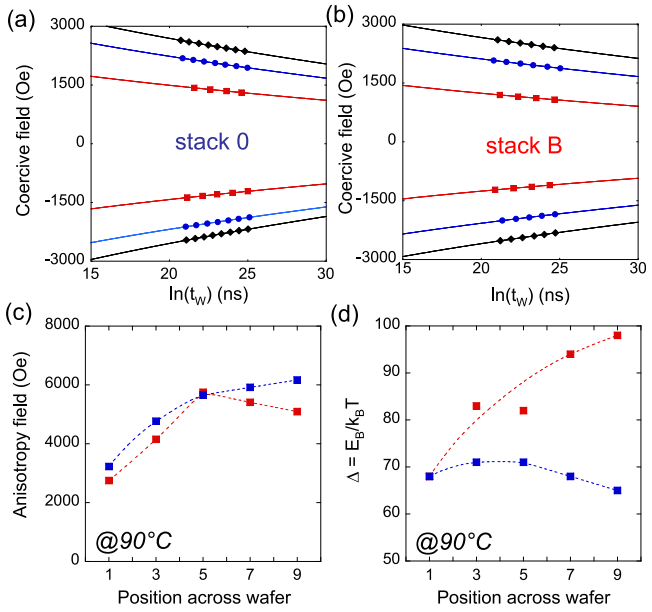

FIG. 8. Time dependent coercivity measurements of 10^6 devices from stack 0 (a) and stack B (b). Solid lines are fits to Eq. (3). Anisotropy field (c) and thermal stability factor (d) as a function stack deposition parameters, which are varied across the wafer. Solid blue and red symbols show data for stack 0 and B, respectively, and dashed lines are guides to the eye. Device median diameter is 45 nm. Experiments are performed at 90 °C.

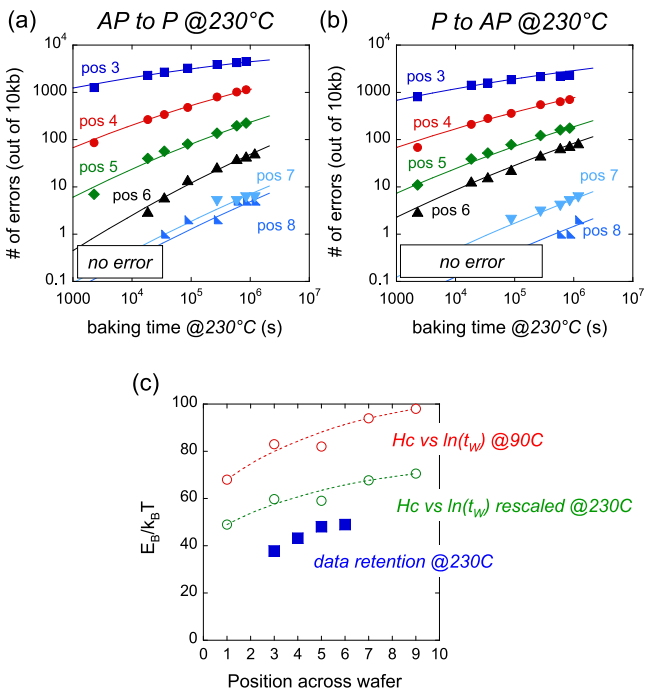

FIG. 9. Data retention experiments performed at 230 °C on 10^4 devices having median diameter of 48 nm. The number of device whose resistance state has changed is recorded as a function of baking time for both AP (a) and P (b) initial states. Solid lines are guides to the eye. The thermal stability factor extracted from this data is shown as solid blue symbols in (c). Open symbols show data from Fig. 8(b).

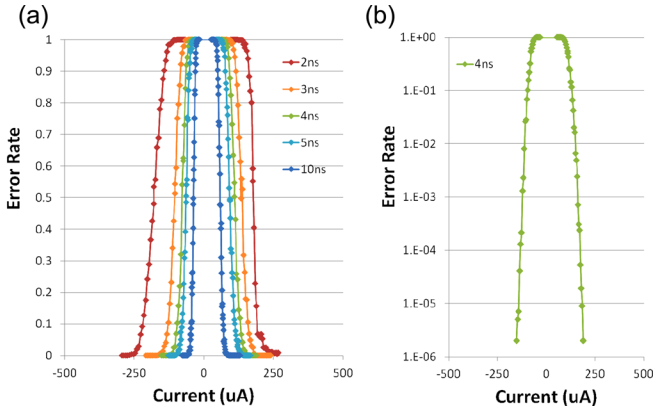

FIG. 10. Bit error rate as a function of current for a 45-nm diameter device in response to nanosecond long current pulses.

position across the wafer (solid blue symbols in Fig. 9(c)). These data point are the mean of the values extracted for of P to AP and AP to P switching (which differ by up to 20%). For comparison, we also show data obtained at 90 °C (open red symbols) as well as the same data rescaled so as to account for the temperature difference (open green symbols). While the two sets of measurements follow the same trend, values derived from measurements at 230 °C are significantly smaller. The difference is likely due to the decrease of anisotropy with temperature.

We now turn to the writing performance our PMA-MTJ devices. Fig. 10 shows the results of a write error test performed on a 45-nm diameter device as a function of the write pulse current for pulse lengths between 2 and 8 ns. No external field is applied in this experiment. The device can be switched reliably with 2 ns pulses. Write error rate smaller than 10^{-6} is achieved for pulses as short as 4 ns, thus showing the potential of our PMA-MTJ stack for high-speed applications.

We have demonstrated that the properties of our PMA-MTJs remain excellent after 90 min anneal at 400 °C. We have also shown good data retention at 230 °C for 48-nm diameter devices. This performance is made possible by the extremely high thermal stability ratio of our devices, which exceeds 120 at room temperature for 45-nm devices. Our PMA-MTJ stacks also exhibit TMR ratio exceeding 150% and high spin torque efficiency. This set of properties makes STT-MRAMs based on our PMA-MTJ stacks ready for production of non-volatile embedded memory for both electronic and automotive applications.

The CMOS chip was designed and built in collaboration with IBM. We thank the IBM-Burlington design team, in particular John DeBrosse and Tom Maffitt for their help with the chip.

[1]S. S. P. Parkin *et al.*, J. Appl. Phys. **85**, 5828 (1999).
[2]S. Tehrani *et al.*, IEEE Trans. Magn. **35**, 2814 (1999).
[3]M. Julliere, Phys. Lett. A **54**, 225 (1975).
[4]S. S. P. Parkin *et al.*, Nature Mater. **3**, 862 (2004).
[5]S. Yuasa, T. Nagahama, A. Fukushima, Y. Suzuki, and K. Ando, Nature Mater. **3**, 868 (2004).
[6]S. Ikeda *et al.*, Appl. Phys. Lett. **93**, 082508 (2008).
[7]M. Durlam *et al.*, Tech. Dig. - Int. Electron Devices Meet. **2003**, 995.
[8]J. DeBrosse *et al.*, IEEE J. Solid State Circuits **39**, 678 (2004).
[9]B. N. Engel *et al.*, IEEE Trans. Magn. **41**, 132 (2005).
[10]J. C. Slonczewski, J. Magn. Magn. Mater. **159**, L1 (1996).
[11]L. Berger, Phys. Rev. B **54**, 9353 (1996).
[12]M. Hosomi *et al.*, Tech. Dig. - Int. Electron Devices Meet. **2005**, 459.
[13]T. Kahawara *et al.*, ICCSC Tech. Dig. **2007**, 480.
[14]R. Beach *et al.*, Tech. Dig. - Int. Electron Devices Meet. **2008**, 305.
[15]S. Chung *et al.*, Tech. Dig. - Int. Electron Devices Meet. **2010**, 12.7.1.
[16]N. D. Rizzo *et al.*, IEEE Trans. Magn. **49**, 4441 (2013).
[17]T. Yamamoto *et al.*, J. Appl. Phys. **97**, 10P503 (2005).
[18]E. Chen *et al.*, IEEE Trans. Magn. **46**, 1873 (2010).
[19]J. Z. Sun, Phys. Rev. B **62**, 570 (2000).
[20]T. Kishi *et al.*, Tech. Dig. - Int. Electron Devices Meet. **2008**, 309.
[21]S. Ikeda *et al.*, Nature Mater. **9**, 721 (2010).
[22]D. C. Worledge *et al.*, Appl. Phys. Lett. **98**, 022501 (2011).
[23]W. Kim *et al.*, Tech. Dig. - Int. Electron Devices Meet. **2011**, 24.1.1.
[24]M. Gajek *et al.*, Appl. Phys. Lett. **100**, 132408 (2012).
[25]G. Jan *et al.*, Appl. Phys. Express **5**, 093008 (2012).
[26]T. M. Maffitt *et al.*, IBM J. Res. Dev. **50**, 25 (2006).
[27]Y. J. Lee *et al.*, Int. Symp. VLSI Technol., Syst., Appl. (VLSI-TSA), Proc. Tech. Pap. **2013**, TR34.
[28]M. T. Johnson, P. H. J. Bloemen, F. J. A. den Broeder, and J. J. de Vries, Rep. Prog. Phys. **59**, 1409 (1996).
[29]W. H. Butler, X.-G. Zhang, T. C. Schulthess, and J. M. MacLaren, Phys. Rev. B **63**, 054416 (2001).
[30]E. J. Marinissen, B. Prince, D. Keitel-Schulz, and Y. Zorian, in *Proceedings of IEEE Computer Society DATE'05*, 2005.
[31]J. Hayakawa, S. Ikeda, Y. M. Lee, F. Matsukara, and H. Ohno, Appl. Phys. Lett. **89**, 232510 (2006).
[32]D. D. Djayaprawira *et al.*, Appl. Phys. Lett. **86**, 092502 (2005).
[33]J. Hayakawa, S. Ikeda, F. Matsukara, H. Takahashi, and H. Ohno, Jpn. J. Appl. Phys., Part 2 **44**, L587 (2005).
[34]P. J. Flanders and M. P. Sharrock, J. Appl. Phys. **62**, 2918 (1987).
[35]X. Feng and P. Visscher, J. Appl. Phys. **95**, 7043 (2004).
[36]R. H. Koch, J. A. Katine, and J. Z. Sun, Phys. Rev. Lett. **92**, 088302 (2004).
[37]W. H. Butler *et al.*, IEEE Trans. Magn. **48**, 4684 (2012).
[38]D. Pinna, A. Mitra, D. L. Stein, and A. D. Kent, Appl. Phys. Lett. **101**, 262401 (2012).
[39]H. Tomita *et al.*, Appl. Phys. Lett. **102**, 042409 (2013).
[40]J. Z. Sun *et al.*, Phys. Rev. B **84**, 064413 (2011).
[41]H. Sato *et al.*, Appl. Phys. Lett. **99**, 042501 (2011).