Self-judgement flip coding for resistive random access memory

Zhongyuan Xiang and Feng Zhang✉

A novel low-energy write scheme, self-judgement flip coding (SJFC), for resistive random access memory (RRAM) is proposed. Lots of energy will be consumed in the write process of RRAM, especially in the reset process. Owing to RRAM being sensitive to heat, excessive heat accumulation will lead to thermal crosstalk. Through reading original data, SJFC analyses and computes the Joule heat produced in the write data flow and further judges whether to make flip coding on the write data flow. The result is that between the original write data flow and flip coding data flow, the one producing lesser energy will be transmitted to the write circuit to produce lesser energy in the RRAM write process. The stimulation result shows that SJFC could reduce energy consumption by 39% on average in the write process.

Introduction: Owing to the limitation in area, power consumption, speed and so on, traditional non-volatile memories, such as FLASH, cannot satisfy the storage needs on a large scale. At the same time, resistive random access memory (RRAM) is considered the most promising emerging memory to take the mainstream position of FLASH due to its excellent characteristics, such as high integration density, low power consumption, high speed in read and write, as well as good compatibility with CMOS process.

Joule heat plays a key role in the process of the formation and the fracture of the RRAM conductive filament [1, 2]. Especially in the reset process, the RRAM unit is in the low resistance state (LRS) initially so that the current is larger than the set process, in which the RRAM unit is in the high resistance state initially, with more Joule heat being generated during the process [3]. Plenty of energy will be consumed in the write process of RRAM and the adjacent RRAM units get closer when RRAM is in high integration density. As heat is conductive and Joule heat is important in the set and reset process of RRAM, excessive Joule heat will lead to state flip, as is similar to over write [1, 4]. When a RRAM unit does the write operation frequently, especially the reset operation, the heat produced will be accumulated and conducted to the adjacent RRAM units. Then the resistive state of adjacent RRAM units will be influenced so that its retention character will get worse and even the resistive state may switch. This is the so-called thermal crosstalk in RRAM.

To reduce the heat produced in the write process of RRAM and weaken the thermal crosstalk, a low-energy write scheme, self-judgement flip coding (SJFC) for RRAM, is proposed.

Self-judgement flip coding: Different from FLASH, RRAM does not need to do an erase operation before writing. Therefore, when the RRAM unit in the LRS is set, that is, write '1' to '1', unnecessary over write will happen. It is similar to writing '0' to '0'. Over write will result in energy waste and even resistance state flip. The essential reason is superabundant Joule heat [1]. The problem mentioned above can be eliminated with the self-adaptive write mode (SAWM) [4] in the write circuit of RRAM. If '1' is written to the RRAM unit which is stored as '1', the write circuit will switch off the write voltage immediately. It is the same with writing '0' to '0'. That is to say, only if the resistance state needs to flip in the write process, the write circuit will add the corresponding write voltage pulse to the RRAM unit, as will lead to the Joule heat generation of the unit. Therefore, the heat produced in the write process of RRAM is related to not only write data, but also the original data in RRAM.

If the assumptions are as follows: the write data flow of n bits is $w[n{:}1]$, w for short, and the original data in the memory is $r[n{:}1]$, r for short; the Joule heat produced in the set per unit is denoted as '1' and the Joule heat produced in reset per unit is denoted as 'k' ($k > 1$); the bitwise not of w is denoted as w' and the bitwise not of r is denoted as r'; Q is the quantity of heat produced after the writing data flow, then Q could be calculated by the formula as follows:

$$Q = k \cdot \sum_{1}^{n} (w' \cdot r) + \sum_{1}^{n} (w \cdot r') \quad (1)$$

where $\sum_1^n (w' \cdot r)$ in (1) denotes the sum of a vector with n bits which is obtained by the inner product of w' and r. Apparently when r is constant, Q depends on w, then we call the bitwise not of w is a flip coding of w. After a flip coding of w, the Q_{flip} produced after the flip coding of the write data flow can be written as

$$Q_{\text{flip}} = k \cdot \sum_{1}^{n} (w \cdot r) + \sum_{1}^{n} (w' \cdot r') \quad (2)$$

Therefore, the flip coding discriminant can be written as

$$Q - Q_{\text{flip}} = \left\{ \begin{array}{l} \left[k \cdot \sum_{1}^{n} (w' \cdot r) + \sum_{1}^{n} (w \cdot r') \right] - \\ \left[k \cdot \sum_{1}^{n} (w \cdot r) + \sum_{1}^{n} (w' \cdot r') \right] \end{array} \right\} \quad (3)$$

If the result of (3) is >0, it indicates that a lesser heat is generated and the heat accumulation effect is weakened, with flip coding.

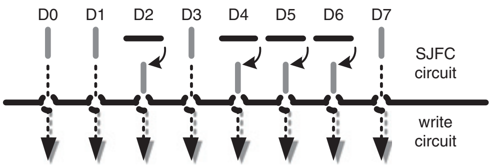

Fig. 1 *Diagram of SJFC*

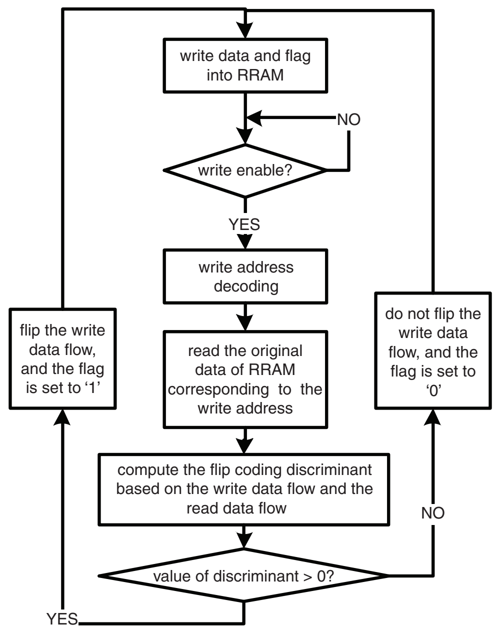

Fig. 2 *SJFC flowchart*

On the basis of the mathematical analysis mentioned above, the SJFC circuit is added before the write circuit of RRAM. Ahead of the write operation of the write circuit, the SJFC circuit reads the data r of the RRAM unit in the memories corresponding to the write operation address. With the calculation of (3) based on r and the write data flow w, SJFC can judge whether to make flip coding of the write data flow. As Fig. 1 shows, if a 64 bits write data flow is divided into eight data blocks called D0 to D7, respectively, and each data block corresponds to 8 bits data, then the SJFC circuit will make discriminant calculation of the flip coding on eight data blocks in parallel. If the result of the discriminant calculation is less than or equal to 0, the data blocks could be transmitted to the write circuit of RRAM directly, such as D0, D1, D3 and D7. Otherwise, data blocks are needed to be made flip coding, like D2, D4, D5 and D6, and only flipped data blocks can be transmitted to the write circuit of RRAM.

Fig. 2 is the flowchart of SJFC. The SJFC circuit chooses the one producing lesser heat between the original and the flip coding data flow, to be transmitted to the write circuit, for the purpose of reducing the Joule heat generated in the write operation of RRAM. The cost of the SJFC scheme is adding a flag bit in each data block to show whether this block has been made flip coding and to guarantee the correct decoding when read in the future. In addition, the SJFC scheme adds the read process in the traditional write process so that the write process will slow down. Fortunately, the time for the read process of RRAM is merely 1/40 of the write process [5], therefore it has little influence on the speed of the write process. What is more, because the time for the read process is so short, its energy consumption is also very limited.

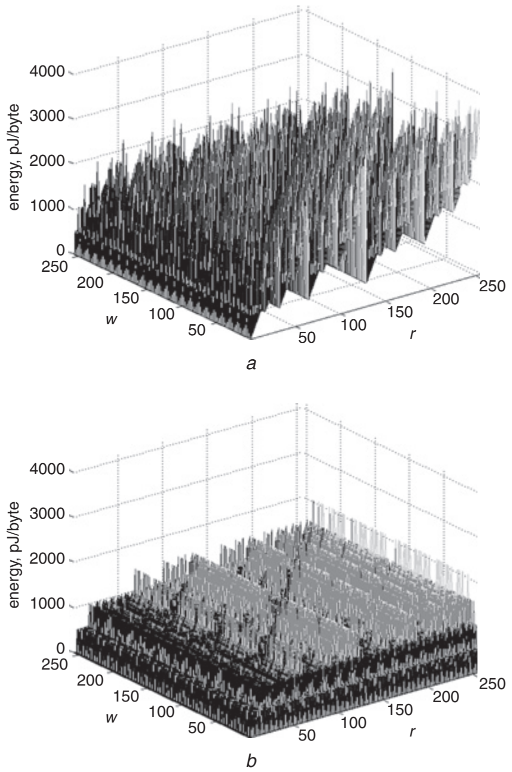

Fig. 3 *Heat simulation results chart*

a Simulation results without SJFC
b Simulation results with SJFC

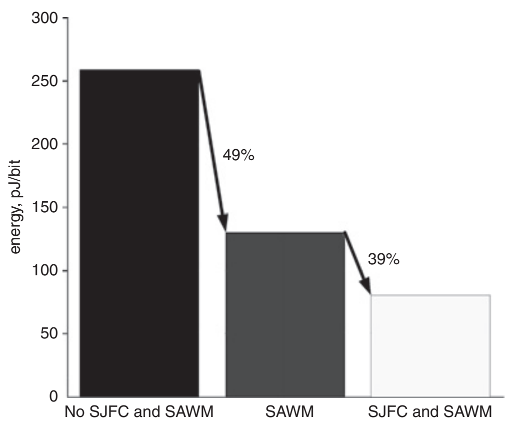

Fig. 4 *Column chart of average power consumption in write process of each RRAM unit*

Simulation results: SJFC was implemented with Verilog HDL and verified with the Synopsys VCS simulation tool. The result data was processed with MATLAB. The calculation of the flip coding discriminant is the key to the SJFC circuit. It is the function of read data flow *r*, write data flow *w*, reset operation Joule heat weight *k* and the bit width of the data block *n*. Byte was chosen to be the unit of the data block, that is, *n* is equal to 8. *k* could be calculated by referring to the energy produced in the reset and set operation in reference paper [4], that is, the energy of the reset operation is 517 pJ/bit and the energy of the set operation is 1.46 pJ/bit, then *k* is about 354.

Fig. 3 is the simulation results chart of heat produced in the write data with byte as the data block. To be specific, *r* is the original storage data in RRAM (0–255) and *w* is the write data flow (0–255). Fig. 3*a* is the stimulation results without the SJFC circuit and Fig. 3*b* is the simulation results with the SJFC circuit. Compared with Fig. 3*a*, the heat shown in Fig. 3*b* is compressed and the quantity of heat is mainly under 2000 pJ/byte.

Fig. 4 is the column chart of the average energy consumption in the write process of each RRAM unit. The simulation results show that 49% heat could be reduced with the adoption of SAWM in the circuit. If the SJFC scheme is adopted, heat could be reduced by 39% on this basis so that the heat in the RRAM could be reduced more wholly.

Remarkably, the simulation results show that with the adoption of SAWM, the value of *k* is about 354; without SAWM, *k* is about 5 [4]. By contrast, *k* is reduced 98%, but the compression ratio of heat with SJFC just reduces about 4%. This indicates that the reduction effect of heat with SJFC does not rely on a large *k*.

The simulations mentioned above are based on the result of a single byte data block, that is, *n* is equal to 8. Designers can adjust this value according to actual needs. Apparently, the smaller the *n* value, the higher will be the reductive percentage of heat. When *n* is 4 and *k* is 8, the average reductive percentage of heat with the adoption of the SJFC scheme could be over 50%. However, the cost is that every 4 bits data requires a flag to indicate whether this bit has been made flip coding. That is, the memory needs 20% storage space to store the flag information, but the scheme with the single byte as the unit of the data block only needs an extra 1/9 storage space. Due to the high integration of the RRAM, the storage space will not be the problem generally, but designers had better set the *n* value based on the actual condition.

Conclusion: A low-energy write scheme based on SJFC is proposed. The result is that between the original write data flow and the flip coding data flow, the one producing lesser energy will be transmitted to the write circuit to produce lesser energy in the RRAM write process. Theoretical analysis and stimulation results show that SJFC could reduce energy by 39% on average in the write process.

Acknowledgments: This work was supported by the 'Key Technology in RRAM Peripheral Circuit Design' Program of the National High-tech R&D Program (863 Program) (no. 2011AA010403), and by the National Natural Science Foundation of China under grant 61474134.

Submitted: *6 July 2015* E-first: *27 November 2015*
doi: 10.1049/el.2015.2332

Zhongyuan Xiang and Feng Zhang (*Institute of Microelectronics of the Chinese Academy of Sciences, Beijing 100029, People's Republic of China*)

✉ E-mail: Zhangfeng_ime@ime.ac.cn

References

1 Chen, Z., Huang, P., Li, H., *et al.*: 'Optimization of uniformity in resistive switching memory by reducing thermal effect'. 12th IEEE Int. Conf. on Solid-State and Integrated Circuit Technology (ICSICT), Hangzhou, China, October 2014
2 Liu, H., Lv, H., Yang, B., *et al.*: 'Uniformity improvement in 1T1R RRAM with gate voltage ramp programming', *IEEE Electron Device Lett.*, 2014, **35**, (12), pp. 1224–1226
3 Ninomiya, T., Muraoka, S., Wei, Z., *et al.*: 'Improvement of data retention during long-term use by suppressing conductive filament expansion in TaO_x bipolar-ReRAM', *IEEE Electron Device Lett.*, 2013, **34**, (6), pp. 762–764
4 Xue, X., Jian, W., Yang, J., *et al.*: 'A 0.13 m 8 MB logic-based Cu_xSi_yO ReRAM with self-adaptive operation for yield enhancement and power reduction', *IEEE J. Solid-State Circuits*, 2013, **48**, (5), pp. 1315–1322
5 Kim, S.Y., Baek, J.M., Seo, D.J., Park, J.K., Chun, J.H., and Kwon, K. W.: 'Power-efficient fast write and hidden refresh of ReRAM using an ADC-based sense amplifier', *IEEE Trans. Circuits Syst. II, Express Briefs*, 2013, **60**, (11), pp. 776–780