Two-bit multi-level phase change random access memory with a triple phase change material stack structure

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This work demonstrates a novel two-bit multi-level device structure comprising three phase change material (PCM) layers, separated by SiN thermal barrier layers. This triple PCM stack consisted of (from bottom to top), $Ge_2Sb_2Te_5$ (GST), an ultrathin SiN barrier, nitrogen-doped GST, another ultrathin SiN barrier, and $Ag_{0.5}In_{0.5}Sb_3Te_6$. The PCM layers can selectively amorphize to form 4 different resistance levels ("00," "01," "10," and "11") using respective voltage pulses. Electrical characterization was extensively performed on these devices. Thermal analysis was also done to understand the physics behind the phase changing characteristics of the two-bit memory devices. The melting and crystallization temperatures of the PCMs play important roles in the power consumption of the multi-level devices. The electrical resistivities and thermal conductivities of the PCMs and the SiN thermal barrier are also crucial factors contributing to the phase changing behaviour of the PCMs in the two-bit multi-level PCRAM device. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4765742]

I. INTRODUCTION

The Flash memory technology faces immense scaling challenges beyond the 10 nm technology node. Therefore, other non-volatile memory (NVM) technologies such as phase change random access memory (PCRAM) have been investigated for possible replacement of the Flash memory.[1–4] PCRAM has become one of the best alternatives to Flash memory because of its fast read, write and erase speeds, high scalability, low power consumption, and its ability to exhibit multi-level behaviour.[5–17] PCRAM also exhibits multi-level characteristics, making it attractive as a contender in high density memory applications required in consumer electronics.[18] As such, investigating the multi-level behaviour in PCRAM cells becomes pertinent, so as to eliminate the problem of resistance drifting.[19] This would in turn propel PCRAM as a forerunner for multi-bit high density storage applications. Resistance drifting is the phenomenon, which has been reported in PCRAM devices with a single phase change layer, where intermediate multi-level resistances were achieved through various programming voltages,[19] and these intermediate resistance levels tend to drift significantly within a short period of time and are thus unstable.

We had previously investigated the feasibility of a dual phase change material (PCM) structure with a thermal barrier layer in between the two PCM layers.[20,21] Three stable multi-level states were achieved, and the problem of resistance drifting was alleviated.[19] The phase changing behaviour of the PCMs in the two-bit multi-level device was also investigated, and it was found that the PCM layers could be selectively amorphized through the application of a voltage pulse (set or reset pulses). These reports, though promising, are not enough to increase the bit-size of the memory device. In this paper, an improved PCRAM device structure comprising three PCM layers (also known as the triple PCM stack structure) is investigated. This work demonstrates the feasibility of a two-bit multi-level device using the triple PCM structure. The electrical performance of the multi-level devices and the physics behind the multi-level phase changing behaviour of the PCMs were investigated.

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II. EXPERIMENT

Four-inch Si substrates with 1 μm thick thermally grown SiO_2 were used as starting substrates. 200 nm of titanium-tungsten (TiW) was deposited and patterned as the bottom electrode [Fig. 1(a)]. A 100 nm thick SiO_2 isolation layer having a 1 μm diameter pore was then formed [Fig. 1(b)]. The triple PCM stack comprising 22 nm of $Ge_2Sb_2Te_5$ (GST), 1 nm of SiN, 22 nm of nitrogen-doped GST (NGST), 1 nm of SiN, and a further 22 nm of $Ag_{0.5}In_{0.5}Sb_3Te_6$ (AIST) was deposited and patterned [Fig. 1(c)]. The NGST layer was formed by sputtering GST from a composite target in a N_2/Ar ambient.[22] The NGST had a nitrogen concentration of 3.5 atomic percent (atm. %). The GST, AIST, and SiN layers were sputtered using composite targets. This triple PCM stack was capped with a 10 nm TiW layer to prevent oxidation of the PCM layers, which may lead to poor device performance. A 100 nm thick SiO_2 layer was then deposited and patterned [Fig. 1(d)]. The top electrode metallization was then performed by depositing and patterning 200 nm of TiW [Fig. 1(e)]. A 365 nm lithography system was utilized for all patterning steps, while a DC Magnetron sputtering tool was used for all the deposition processes. Figs. 1(a) to 1(e) summarize the fabrication process flow using cross-sectional schematics.

III. RESULTS AND DISCUSSION

A. Electrical characterization

Fig. 2 displays the resistance-time plot of a particular two-bit multi-level PCRAM device. All electrical readings in this plot as well as all the other plots in this work were

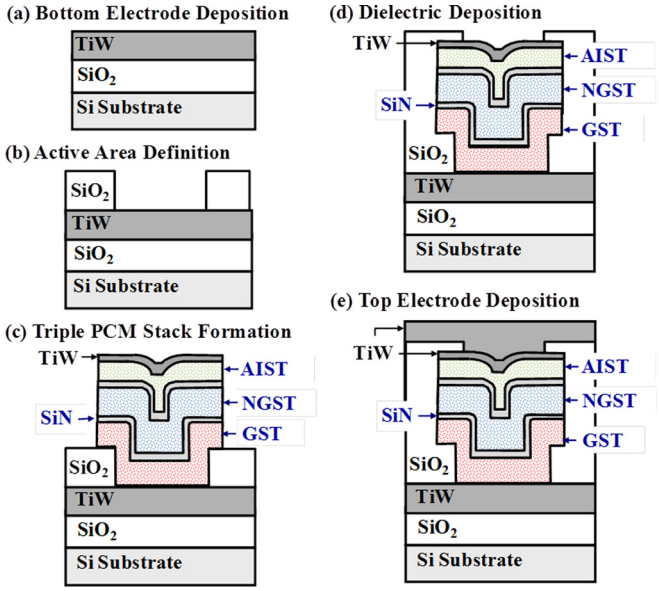

FIG. 1. Process flow for fabrication of PCRAM device having a triple PCM structure. (a) Bottom electrode (200 nm of TiW) formation. (b) Active area definition after deposition of 100 nm of SiO_2 dielectric. (c) Triple PCM stack formation by sequential deposition of 22 nm of GST, 1 nm of SiN, 22 nm of NGST, 1 nm of SiN, 22 nm of AIST, and 10 nm of TiW. (d) 100 nm of dielectric deposition. (e) Top metallization (200 nm of TiW).

obtained using a constant read voltage of 0.2 V and were performed at room temperature and pressure. A current compliance of 0.01 A was also set for all DC and programmable pulse measurements in this work. The four states are clearly annotated in the plot. State I has the lowest resistance value and can also be viewed as being in the "00" state in the two-bit device. State II ("01") has the next highest resistance value, followed by state III ("10"), and the highest resistance state, state IV ("11"). The two-bit multi-level device switches instantaneously at the onset of a voltage pulse. The instants when pulses were applied are indicated by the arrows in Fig. 2. The state II reset pulse (20 ns and 3.2 V) switches the device to state II. The state III reset pulse (20 ns and 4 V) switches the device to state III. The state IV reset pulse (20 ns and 5 V) switches the device to state IV. The state I set pulse (800 ns and 2 V) switches the device to state I. The total resistance (R_{total}) of the device in any state can be written as

$$R_{total} = R_{contact} + 2R_{SiN} + R_{GST} + R_{NGST} + R_{AIST} + 2R_{TiW}, \quad (1)$$

where $R_{contact}$ is the contact resistance of both the TiW electrodes, R_{SiN} is the resistance of each of the SiN thermal barrier layers in the triple PCM stack, R_{GST} is the resistance of the GST layer, R_{NGST} is the resistance of the NGST layer, R_{AIST} is the resistance of the AIST layer, and R_{TiW} is the resistance of each of the electrodes. $R_{contact}$, R_{SiN}, and R_{TiW} remained constant throughout the switching process, however, R_{GST}, R_{NGST}, and R_{AIST} change with respect to the phase of the respective PCMs, thereby changing R_{total}. This change in R_{total} after application of the pulses is depicted in Fig. 2.

The resistance-time plot in Fig. 2 shows that the pulses switch the devices to their respective states from any arbitrary state. This means that the final state does not depend on the resistance of the previous state but on the magnitude and duration of the pulse. It is also important to note at this juncture, that the pulsing method employed to switch the devices throughout the course of the work was the amorphization method as it allows for greater versatility to switch from one state to another.[20] The resistance windows between consecutive states (i.e., the difference in R_{total} between consecutive states) in the device shown in Fig. 2, are large of roughly an order in magnitude.

Fig. 3 displays the retention characteristics of the same two-bit multi-level device illustrated in Fig. 2. The pulsing conditions used to switch the device to its respective states are also annotated in the plot. The device shows excellent retention capabilities as all four multi-level states do not experience any substantial resistance drifting over time. This means that the four multi-level states are stable and would not overlap over time, thus ensuring the ease of programming of these multi-level states. The drift phenomenon is known to occur in PCM devices.[23–25] This is due to the

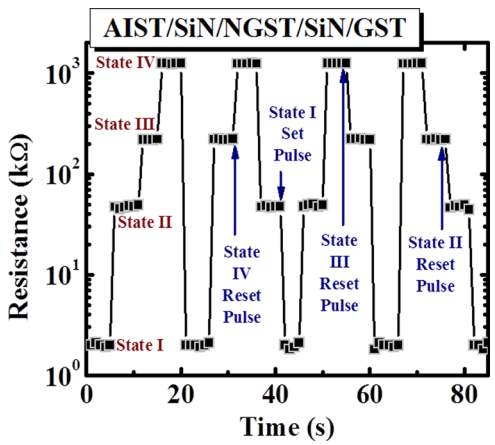

FIG. 2. Resistance-time plot showing the four states in a two-bit multi-level PCRAM device. The onset of the Reset and Set pulses are indicated by the vertical arrows. The resistance states (I, II, III, and IV) are also annotated in the graph.

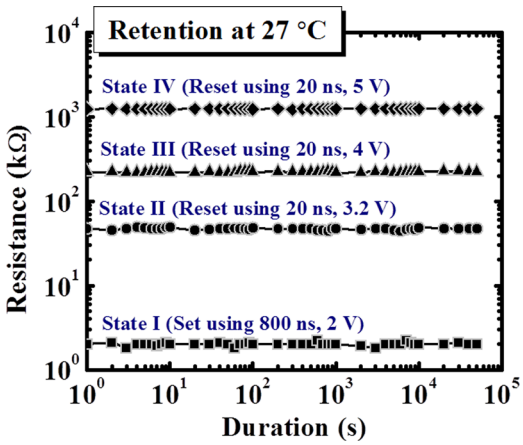

FIG. 3. Retention plots of the same two-bit multi-level device as in Fig. 2. The measurement was performed at room temperature. The pulse conditions used to switch the device to a particular state are also annotated in the graph. The device shows good retention for all four states.

structural relaxation of the amorphous PCM. In multi-level programming of a single-layer PCM device, this drift phenomenon becomes detrimental to multi-level storage as the intermediate resistance levels tend to overlap with the adjacent levels. The excellent retention capabilities of this 2-bit PCM device could be attributed to the intermediate SiN layers. These SiN barrier layers could have greatly reduced structural relaxation in the mostly amorphized PCM layers, since there are negligible poly-crystalline PCM regions surrounding the amorphous PCM regions.

The U-curve in Fig. 4 shows the set and reset operations of another two-bit multi-level device. A fixed pulse width of 800 ns and a variable pulse voltage (horizontal scale in Fig. 4) were used to program the device for each reading. Before each reading was obtained, the device was completely reset back to the highest resistance state, state IV. All four multi-level states can be distinctly differentiated in this resistance-voltage plot. The resistance windows between consecutive states are large (roughly an order of magnitude) and can be clearly observed in Fig. 4. This plot also illustrates the two ways in achieving the four multi-level states (i.e., the crystallization method and the amorphization method). The crystallization method entails setting the device from the highest resistance state till the lowest resistance state is attained.[20] A reset pulse would then be needed to completely reset the device back to state IV. The amorphization method entails the resetting of the device from state I all the way to state IV and then applying a set pulse to switch the device back to state I.[20] As mentioned earlier, the switching of the device from one state to another in this work was done through the amorphization method, which uses a variety of reset pulses to increase the resistance of the device, and a set pulse to completely set the device back to state I. This is because the amorphization method allows for versatility in switching the device from one state from any arbitrary state, whereas the crystallization method involves the switching of the device in sequence (i.e., the device can only switch to a particular state from one other state). The multi-level phase changing behaviour of the PCMs, using the amorphization method, will be further discussed in the thermal analysis section.

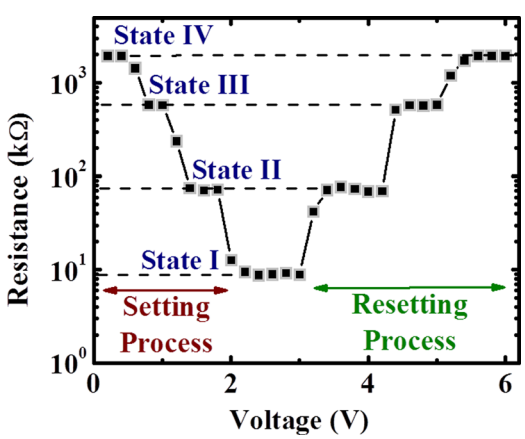

FIG. 4. U-curve of a two-bit multi-level PCRAM device. The set and reset operations are indicated on the graph. The measurements were performed with a constant pulse width of 800 ns, and the pulse magnitude is shown on the horizontal scale. The device was reset back to the highest resistance level (state IV) before each measurement or data point was taken. The four multi-level states (states I, II, III, and IV) are stable and distinct.

Fig. 5 portrays the statistical distribution of the respective resistance states for a set of 10 measured devices. This plot shows that the resistance values in each state are relatively well separated. It can be clearly seen that there are no overlaps between consecutive states. This allows for the ease of programming as there would be no overlapping states from one device to another.

Fig. 6 displays the endurance characteristics of another two-bit multi-level PCRAM device. The four reset and set pulses were applied in the following order: state II reset pulse, state III reset pulse, state IV reset pulse, and state I set pulse. Each cycle consisted of resistance values recorded after the application of the four reset and set pulses in the aforementioned sequence. The extrapolated endurance plot (dashed lines) shows that the device can last for longer than 10^7 cycles while maintaining the large resistance windows between consecutive states. This means that the device has the potential for high endurance (i.e., $\sim 10^9$ cycles). Another important point to note is that the resistance windows between consecutive states are constant and stable, maintaining the one order difference between consecutive states throughout the endurance testing. This shows that the two-bit device shows potential for use in high-density storage applications.

B. Thermal analysis

To investigate the two-bit multi-level phase changing behaviour of the PCMs, the Joule heat distribution in each PCM layer of the two-bit multi-level PCRAM device was investigated using a two-dimensional finite element simulation. The material properties used in this simulation were assumed to be temperature invariant and isotropically homogeneous. The voltage pulse was applied to the top electrode during this Joule heating simulation.[26] The thermal transfer process in this simulation follows the standard heat conduction equation:

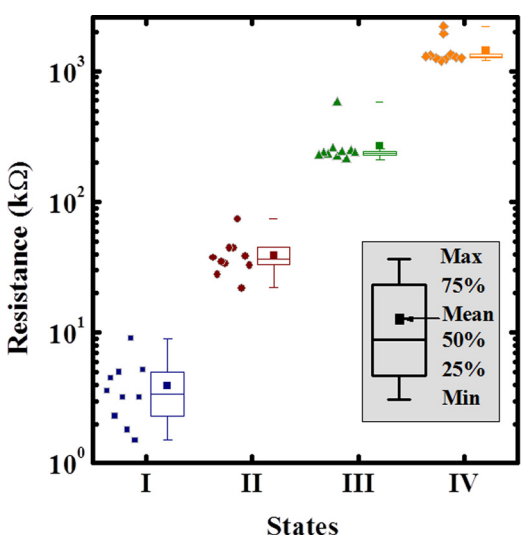

FIG. 5. Box plots illustrating the distribution of resistance values for each state for a set of 10 measured devices. The devices show tight distributions of resistance values for each state.

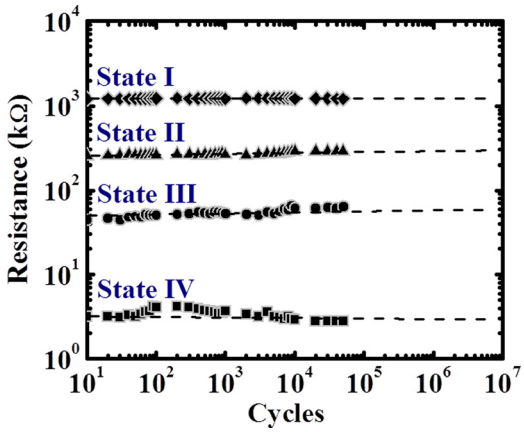

FIG. 6. Endurance cycles of a two-bit multi-level device (indicated by the data points). The dashed lines illustrate the extrapolated endurance of the device to 10^7 cycles. The device shows good potential for high endurance. The resistance states are very stable, and the resistance windows are consistently large.

$$\nabla \cdot k\nabla T + Q = c\rho \frac{\partial T}{\partial t}, \tag{2}$$

where ∇ is the gradient operator, k is the thermal conductivity, T is the temperature, Q is the Joule heat per unit volume and time, c is the specific heat capacity, ρ is the density, and t is the time.[27] All four voltage pulses were simulated to determine the temperature distribution in each PCM layer for the amorphization method of switching. Two additional voltage pulses were simulated to compare the amorphization method with the crystallization method of switching. This is critical so as to understand how both the PCM layers change phase with respect to typical set and reset voltage pulses. The temperature profile plots in Figs. 7 to 11 were extracted from peak temperature nodes in each of the PCM layers. The boundary conditions at the top surface of the top electrode and the bottom of the 1 μm thick SiO_2 (on the Si wafer) were set to be at room temperature (27 °C). All temperature conditions in the device were also initialized to be at room temperature (27 °C) before each voltage pulse simulation. The melting (T_M) and crystallization (T_C) temperatures, as well as the electrical resistivity and thermal conductivity of the materials used in the triple PCM stack are included in Table I for reference. It should also be noted that the respective PCM can only amorphize when the temperature rises above its T_M in a fast melt-quench process (in the order of tens of nanoseconds), whilst the PCM crystallizes once its temperature is in between its respective T_M and T_C for a longer duration (in the order of hundreds of nanoseconds). The fast melt-quench process prevents the PCM molecules from arranging in an ordered fashion, thus amorphizing the PCM. The longer crystallization pulse, on the other hand, allows the PCM molecules to be arranged in a more orderly fashion, thereby crystallizing the PCM.

Fig. 7(a) shows the simulated temperature versus time profiles during and after the application of the state II reset pulse (20 ns and 3 V). The curves (labelled as 1, 2, and 3) were obtained by plotting the temperatures of the correspondingly numbered nodes in Fig. 7(b). These nodes are roughly in the middle of each PCM layer in the triple PCM

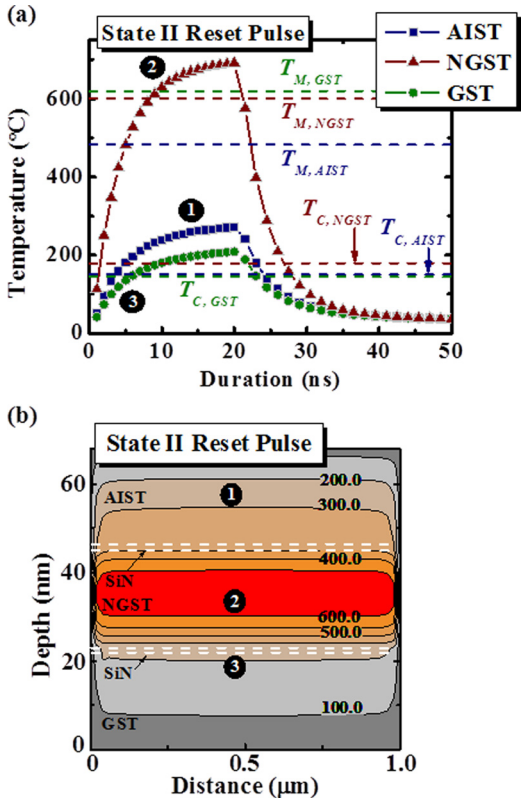

FIG. 7. (a) Simulated temperature versus time profiles of a two-bit multi-level device undergoing the state II reset pulse (20 ns and 3 V). The voltage pulse was applied from 0 to 20 ns. The temperature in AIST (plotted as square symbols), NGST (plotted as triangle symbols), and GST (plotted as circle symbols) were taken at points 1, 2, and 3, respectively, as indicated in (b). (b) Simulated temperature contour plot of the two-bit multi-level device undergoing the same state II reset pulse, taken at 20 ns after application of the pulse. The temperature versus time profiles, in (a), were extracted from the nodes labelled 1, 2, and 3.

stack. Fig. 7(b), on the other hand, shows the simulated temperature contour of the PCM device during the state II reset pulse. The nodes at which the temperature versus time graphs were extracted from [in Fig. 7(a)] are labelled as 1, 2, and 3. During the state II reset pulse, the temperature in the NGST layer exceeds its T_M (600 °C) and amorphizes upon rapid cooling, hence increasing R_{NGST}. The temperatures in the AIST and GST layers, however, are in between their T_M and T_C (as seen in Table I) and thus are poly-crystalline. The combination of amorphous NGST, and poly-crystalline AIST and GST forms one of the intermediate resistance levels, state II. It should be noted that this state II reset pulse can switch the device to state II regardless of the previous state. This is because every time the state II reset pulse is applied, the temperatures in the PCMs would rise such that in NGST exceeds its T_M, while those in AIST and GST remain in between their T_M and T_C. The temperature in the NGST shoots up to a higher level than its T_M first as the NGST is bounded by the thermal barrier SiN layer, which has a much lower thermal conductivity than the NGST layer (indicated in Table I). This means that the heat generated is trapped within the NGST layer, causing its temperature to rise more rapidly.

The simulated temperature versus time profiles during the state III reset pulse (20 ns and 4.5 V) are shown in

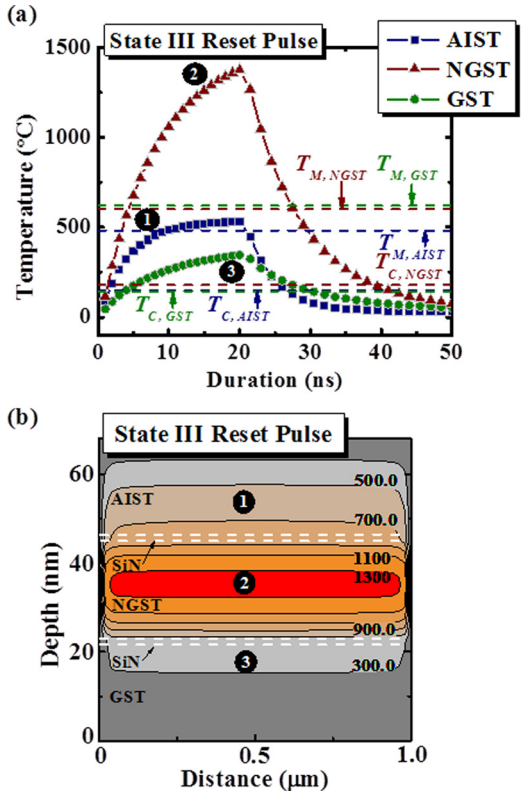

FIG. 8. (a) Simulated temperature versus time profiles of a two-bit multi-level device undergoing the state III reset pulse (20 ns and 4.5 V). The voltage pulse was applied from 0 to 20 ns. The temperature in AIST (plotted as square symbols), NGST (plotted as triangle symbols), and GST (plotted as circle symbols) were taken at points 1, 2, and 3, respectively, as indicated in (b). (b) Simulated temperature contour plot of the two-bit multi-level device undergoing the same state III reset pulse, taken at 20 ns after application of the pulse. The temperature versus time profiles, in (a), were extracted from the nodes labelled 1, 2, and 3.

Fig. 8(a). The curves (labelled as 1, 2, and 3) were obtained by plotting the temperatures of the correspondingly numbered nodes in Fig. 8(b). These nodes are roughly in the middle of each PCM layer in the triple PCM stack. Fig. 8(b) illustrates the simulated temperature contour of the two-bit device during the state III reset pulse. The nodes at which the temperature versus time graphs were extracted from [in Fig. 8(a)] are labelled as 1, 2, and 3. During the state III reset pulse, the temperatures in both the NGST and the AIST layers rise above their respective T_M, and become amorphous upon cooling. This means that both R_{NGST} and R_{AIST} increase in value. The temperature in the GST layer, however, still remains in between its T_C and T_M. Thus, the GST layer becomes poly-crystalline. The temperature in the NGST layer escalates to a high temperature quickly due to the thermal insulation provided by the SiN at the top and bottom of the NGST layer. This time, the AIST layer also manages to amorphize, despite having similar thermal conductivity as GST (indicated in Table I). This is because the AIST has a relatively lower T_M amongst the three PCMs used in this work. Hence, AIST is able to amorphize after the application of the state III reset pulse. This combination of amorphous AIST and NGST, and poly-crystalline GST forms another one of the intermediate states, state III.

TABLE I. The thermal conductivities (κ) and electrical resistivities (ρ) of as-deposited amorphous PCMs and SiN used in this work. Melting temperatures (T_M) and crystallization temperatures (T_C) of the PCMs are also listed.

Properties	GST	AIST	NGST	SiN
Melting temperature, T_M (°C)[a]	620	607	600	—
Crystallization temperature, T_C (°C)[a]	145	150	180	—
Thermal conductivity, κ (W/mK)[b]	0.3	0.34	0.17	0.075
Electrical resistivity, ρ (Ωm)[c]	5.88	0.45	140	10^9

[a]Melting and crystallization temperatures are taken from Refs. 28–32.
[b]Thermal conductivities are taken from Refs. 33–37. Thermal conductivity of SiN is that of ultrathin SiN.
[c]Electrical resistivities are taken from Refs. 38–44. The electrical resistivity of SiN is that of ultrathin SiN, and those of the PCMs are those of amorphous resistivities.

The simulated temperature versus time profiles during the state IV reset pulse (20 ns and 6 V) are illustrated in Fig. 9(a). The curves (labelled as 1, 2, and 3) were obtained by plotting the temperatures of the correspondingly numbered nodes in Fig. 9(b). These nodes are roughly in the middle of each PCM layer in the triple PCM stack. Fig. 9(b) shows the simulated temperature contour of the two-bit PCM device during the state IV reset pulse. The nodes at which the temperature versus time graphs were extracted from [in Fig. 9(a)] are labelled as 1, 2, and 3. During the state IV reset

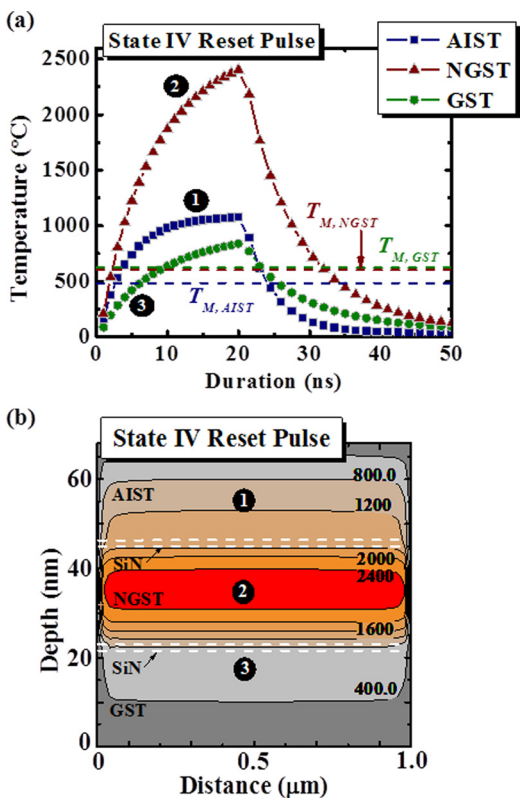

FIG. 9. (a) Simulated temperature versus time profiles of a two-bit multi-level device undergoing the State IV reset pulse (20 ns and 6 V). The voltage pulse was applied from 0 to 20 ns. The temperature in AIST (plotted as square symbols), NGST (plotted as triangle symbols), and GST (plotted as circle symbols) were taken at points 1, 2, and 3, respectively, as indicated in (b). (b) Simulated temperature contour plot of the two-bit multi-level device undergoing the same state IV reset pulse, taken at 20 ns after application of the pulse. The temperature versus time profiles, in (a), were extracted from the nodes labelled 1, 2, and 3.

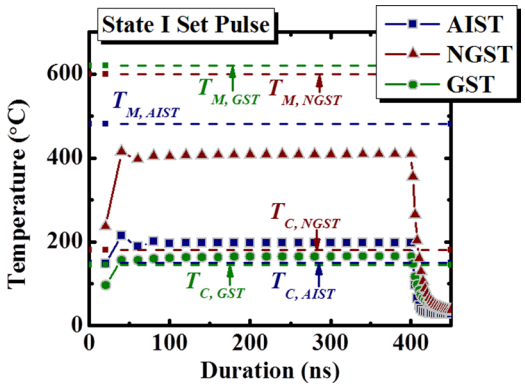

FIG. 10. Simulated temperature versus time profiles of a two-bit multi-level device undergoing the state I set pulse (400 ns and 2 V). The temperature profiles were extracted from nodes roughly in the middle of the GST (circle symbols), NGST (triangle symbols), and AIST (square symbols) layers.

pulse, the temperatures in all three PCMs rise to above their respective T_M (indicated in Table I) and amorphize due to the fast melting and quenching process. The temperature in NGST is exceptionally higher than those in AIST and GST and this can be again attributed to the thermal insulation provided by the SiN thermal barrier layers at the top and bottom of the NGST layer. All three amorphous PCMs form the highest resistance level, state IV where the R_{AIST}, R_{NGST}, and R_{GST} are at their highest values.

Fig. 10 shows the simulated temperature versus time profiles during the state I set pulse (400 ns and 2 V). The temperature plots were extracted from peak temperature nodes in each of the PCM layers. The temperatures of all three PCMs in this plot lie in between their respective T_C and T_M. Hence, all three PCMs become poly-crystalline during the state I set pulse. This means that the Joule heating in the three PCMs is high enough to undergo crystallization. The combination of the three poly-crystalline layers form the lowest resistance state, state I.

The simulated temperature versus time profiles in Fig. 11 represent the crystallization method of switching. In this method, the two intermediate pulses that switch the device to the intermediate resistance states (i.e., states II and III) crystallize the PCM layers instead of amorphizing them (as in the case when the state II reset and state III reset pulses are applied). Thus, the state IV reset pulse switches the device to state IV, the state III set pulse switches the device to state III, the state II set pulse switches the device to state II, and the state I set pulse switches the device to state I. Fig. 11(a) shows the temperature versus time profiles extracted from nodes roughly in the middle of each of the PCM layers, during the state III set pulse (400 ns and 1 V). During this state III set pulse, the temperature in the GST layer lies in between its T_C and T_M, while those in the AIST and NGST layers lie below their respective T_C. This means that the GST layer is able to crystallize first due to its low T_C (as compared to the other two PCMs); whereas, the AIST and NGST layer do not change phase and remain in the states, which they were in before the pulsing event. Herein lies the limitation of the state III set pulse. Unlike, the state II and state III reset pulses, the state III set pulse cannot switch the device to state

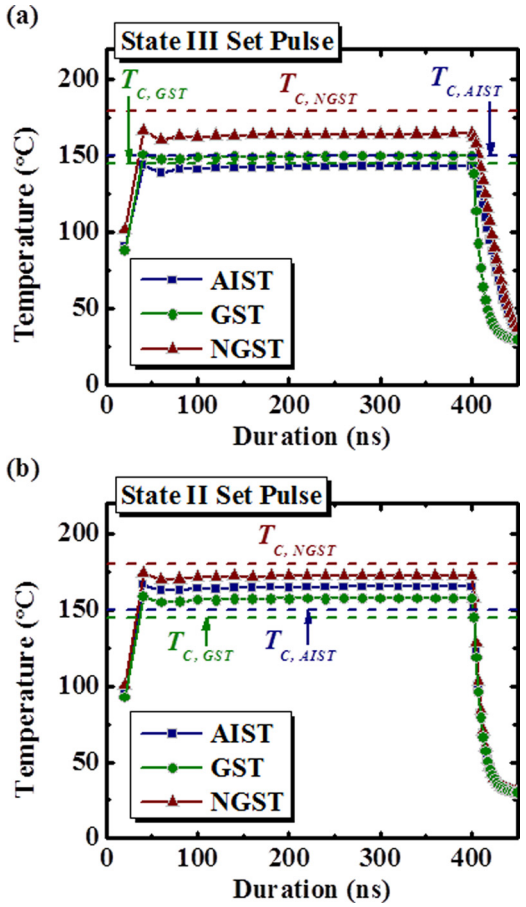

FIG. 11. Simulated temperature versus time profiles of a two-bit multi-level device undergoing the (a) state III set pulse (400 ns and 1 V), and (b) state II set pulse (400 ns and 1.5 V). The temperature profiles were extracted from nodes roughly in the middle of the GST (circle symbols), NGST (triangle symbols), and AIST (square symbols) layers.

III, unless the state prior to the pulsing event is in state IV. Similarly, the temperature profile plots of the three PCM layers during the state II set pulse (400 ns and 1.5 V) is shown in Fig. 11(b). The temperatures in GST and AIST are seen to be in between their T_C and T_M, whereas, that in NGST is not above its T_C. This means that GST and AIST layers become poly-crystalline whereas the NGST remains in the same phase before the pulsing event. The GST and AIST layers are able to crystallize before the NGST layer as their T_C are lower than the T_C of NGST. Thus, the state II pulse can only switch the device to state II if the state prior to the pulsing event was state III.

Fig. 12 is a schematic of the overall two-bit phase changing behaviour of the three PCMs, using the amorphization method. The state II reset pulse amorphizes the NGST layer, while the AIST and GST layers remain poly-crystalline. This combination of amorphous NGST, and poly-crystalline AIST and GST forms state II. The state III reset pulse amorphizes both NGST and AIST, while GST is poly-crystalline. This forms state III. The state IV reset pulse amorphizes all three PCM layers forming the highest resistance level, state IV. The state I set pulse crystallizes all the PCM layers to form the lowest resistance level state I. As discussed earlier, the crystallization method pulses were not reflected in this schematic as the amorphization method

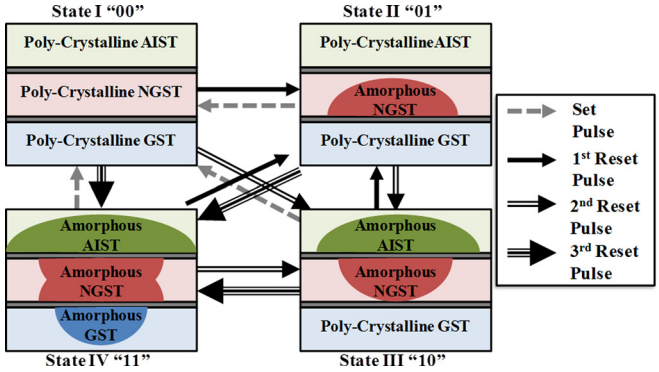

FIG. 12. Schematic of the phase changing process of the three PCMs in a triple PCM mulit-level device (using the amorphization method). The state II reset pulse switches the device to state II, the state III reset pulse switches the device to state III, the state IV reset pulse switches the device to state IV, and the state I set pulse crystallizes the device back to state I. The device can switch to a particular state from any arbitrary state using the respective set or reset pulse.

pulses were a better option. The pulses can switch to a particular state, irrespective of the previous state (as indicated by the arrows in Fig. 12). This independent nature of switching allows the two-bit multi-level device to be programmed with ease without having to go through the switching of states sequentially.

The choice of the PCMs and the sequence of the PCMs in the triple stack structure largely depend on the T_M and T_C of the PCMs. The heat generated in this two-bit multi-level PCRAM device structure is confined within the middle PCM layer. Hence, the middle PCM layer should have the lowest T_M, such that a relatively low voltage pulse could be used to selectively amorphize the middle PCM layer alone. NGST was thus chosen as the middle PCM layer in this work due to its inherently low T_M (as indicated in Table I).

The top and bottom PCM layers in the triple PCM stack were chosen according to their respective T_M as well. The central confinement of heat in this triple PCM stack structure allows the joule heat generated to radiate in an outward fashion. Hence, the PCM with the lower T_M in the top or bottom of the triple PCM stack would amorphize before that with the higher T_M. In this work, the PCM with the lower T_M (i.e., AIST) was used as the top PCM layer, whilst the PCM with the higher T_M (i.e., GST) was used as the bottom PCM layer. The top and bottom PCM layers are interchangeable as the selective amorphization of the bottom and top PCM layers can still be accomplished if the top and bottom PCM layers were swapped. The thermal conductivity of the PCM layers in the top and bottom of the triple PCM stack would determine the heat flux within the PCM layers. The AIST and GST materials used in this work have relatively similar thermal conductivities (as seen in Table I); thus, the heat flux within the top and bottom PCM layers are roughly similar. Moreover, the SiN thermal barrier layers in the triple PCM stack prevent the heat flux in the triple PCM stack to spread to the top and bottom layers too quickly. This damping of heat flux allows the three PCM layers to be amorphized gradually upon the application of higher voltage pulses. Thus, the T_M plays a more crucial role in determining which PCM layer selectively amorphizes first.

The difference in T_M of the three PCMs in the triple PCM stack are hence, crucial in engineering the two-bit multi-level device such that it can switch at lower voltage pulses; this in turn lowers the power consumption of the device. This flexible method of choosing the PCMs to be used in the two-bit multi-level PCRAM structure works when the amorphization method is employed to switch the devices.

IV. CONCLUSION

A novel two-bit multi-level PCRAM device comprising of a triple PCM stack was demonstrated in this work. This triple PCM stack consisted of GST, NGST, and AIST with SiN thermal barrier layers separating the three PCM layers. Electrical characterization was performed to determine the two-bit multi-level device behaviour. Four states (i.e., "00," "01," "10," and "11") were achieved. Resistance windows, between consecutive states, of at least 1 order were realized. The two-bit devices also showed excellent potential for high endurance and showed good retention characteristics. The stability and endurance of the multi-level devices are suitable for high density storage applications. Thermal analysis was also performed to understand the phase changing behaviour of the PCMs in the two-bit multi-level device. The physics behind this phase changing behaviour of the PCMs in the multi-level PCRAM devices was explained.

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