www.ietdl.org

Published in IET Microwaves, Antennas & Propagation
Received on 11th August 2010
Revised on 11th January 2011
doi: 10.1049/iet-map.2010.0388

Special Issue on RF/Microwave Communication Subsystems for Emerging Wireless Technologies

ISSN 1751-8725

60 GHz wide tuning range SiGe bipolar voltage controlled oscillator for high definition multimedia interface and wireless docking applications

G. Huang V. Fusco

High Frequency Electronic Circuits Laboratories, ECIT, Queen's University Belfast, Belfast, UK
E-mail: huangguochi_hit@hotmail.com

Abstract: A wide tuning range voltage controlled oscillator (VCO) with novel architecture is proposed in this work. The entire circuit consists of a VCO core, a summing circuit, a single-ended to differential (STD) converter and a buffer amplifier. The VCO core oscillates at half the desired frequency and the second harmonic of the VCO core is extracted by the summing circuit, which is then converted to a differential pair by the STD. The entire VCO circuit operates from 58.85 to 70.85 GHz with 20% frequency tuning range. The measured VCO gain is less than 1.6 GHz/V. The measured phase noise at 3 MHz offset is less than −78 dBc/Hz across the entire tuning range. The differential phase error of the output signals is measured by down converting the VCO output signals to low gigahertz frequency using an on-chip mixer. The measured differential phase error is less than 8°. The VCO circuit, which is constructed using 0.35 μm SiGe technology, occupies 770 × 550 μm^2 die area and consumes 62 mA under 3.5 V supply.

1 Introduction

Owing to the intrinsic characteristics of short wave length and high attenuation in air, the unlicensed *V*-band frequencies at 60 GHz are currently being adopted for ultrahigh data rate and short-range application, for instance for wireless high definition multimedia interface (HDMI) and wireless docking station [1]. For example, in the European standard [1], the operation frequency band is from 57 to 66 GHz with nearly 9 GHz bandwidth. Such a wide band requirement is very challenging for front end transceiver design, because every block in the system should have enough bandwidth to accommodate the incoming signal. In the transceiver system, one of the most important and complex blocks is the phase-locked loop (PLL), which serves as local oscillator (LO) to the mixing circuit to up/down convert the modulated carrier signal. In addition to the requirement for wide operation frequency tuning range, the PLL should have exhibit low spurious tone response so as not to deteriorate the signal-to-noise ratio (SNR) in wide band systems [2, 3]. Obviously, a wideband low gain voltage controlled oscillator (VCO) is a pre-requisite for the construction of such a demanding PLL system [2, 3].

Many wideband techniques are available in the literature, for instance the switched transmission line method in [4] and the active inductor technique in [5, 6]. However, the switched transmission line method employs many transmission lines in the VCO resonating core and consequently requires large die area. Alternatively, active inductors have limited self-resonant frequency, which constrains their application at millimeter wave (MMW) frequencies. Therefore these two techniques are not preferable for low-cost millimetre wave applications.

However, a technique utilising the second harmonic of the VCO core could be attractive for deployment in the millimeter wave frequency band, because the VCO core needs only to oscillate at half of the desired frequency so that the trade-off among phase noise, frequency tuning range and power dissipation is alleviated.

One example using the second harmonic technique is the so-called push–push oscillator that extracts the second harmonic at the drain node of the tail current source in the VCO core [7–10]. In this kind of oscillator the output signal is single-ended. However, in many cases differential signals are required in transceiver systems because of their high immunity to common mode noise [11]. Thus the single-ended signal must be necessarily converted to a differential pair for millimeter wave frequency use. Although this approach is challenging, it is still worthwhile to further investigate its potential.

Two different balun circuits that can realise single-ended to differential (STD) conversion are available: passive and active. The passive balun is very popular in traditional monolithic microwave integrated circuit design [12], but its insertion loss becomes prohibitive as operation frequency increases [12, 13]. Also, the passive balun is size hungry. The active balun has lower insertion loss and occupies smaller die area. Therefore it is more and more popular to adopt active balun at millimeter wave frequency for the purposes of signal conversion and measurement.

In this paper the second harmonic signal is utilised in order to generate the desired frequency band using a summing

circuit. This approach is fundamentally different from the technique deployed in a push–push topology. In this paper a switched varactor array is introduced in order to obtain low gain wide tuning range performance since this is one of the most effective techniques to reduce VCO gain [14]. An active STD converter is also adopted in order to create a differential pair. The differential phase error at the VCO outputs is measured by integrating an on-chip down-convert mixer together with the VCO. The proposed wideband VCO is described in Section 2. The measurement results are illustrated in Section 3. Finally conclusions are shown in Section 4.

2 Design of the 60 GHz wide tuning range SiGe VCO

The block diagram of the proposed wide tuning range VCO is shown in Fig. 1*a*. The entire circuit consists of four blocks: a VCO core, a summing circuit, a STD converter and a differential cascode amplifier. The VCO core is designed to oscillate at ω_0. The output signals of the VCO core are summed together using two capacitors C_9 and C_{10}. Thus the even harmonics are extracted and all odd harmonics are cancelled. As a result the second harmonic emerges at the output port of the summing circuit. However, this signal is single-ended. Thus an STD circuit is employed to convert the single-ended signal to a differential pair since in many transceiver systems a differential signal is preferred. The differential cascode amplifier is adopted to further amplify the desired signal and improve the phase and amplitude balances of the STD output signals.

There are three varactor banks, C_{v1} to C_{v3}, among which two are used for coarse frequency tuning and the other, C_{v1}, is used for continuous fine tuning. C_5 and C_6 are used as direct current (DC) blocking capacitors. R_2 and R_3 provide DC feed-through path for the PN junction varactor diodes. Customised spiral inductors, L_{1-2}, are simulated in HFSS and modelled using a double-π equivalent resistor inductor and capacitor network (RLC) circuit [15]. The simulated inductance and quality factor (Q-factor) at 30 GHz are about 142 pH and 24, respectively. The simulated Q-factor of the variable capacitor banks, which includes three varactor group C_{V1-3}, two DC blocking capacitors C_{5-6}, and two DC feeding resistors R_{2-3}, are each about 6.5 at 30 GHz. Thus, the phase noise performance of the VCO is primarily determined by the varactor diodes. Transistor Q_{1-2} and capacitors C_{1-4} form a negative resistance designed to compensate for the loss in the inductor and capacitor network (LC) tank. A common emitter (CE) amplifier with series RL load serves as a buffer stage to alleviate the capacitive load of the VCO core. The single-ended second harmonic signal is extracted by a summing circuit, constructed by C_9 and C_{10}, and converted to a differential pair by a STD converter [16]. The output of the summing stage is injected into the base of Q_6. A partial output signal of Q_6 is fed back to the base of Q_7 by using C_{11} to connect Q_7 base node with Q_6 collector node. This approach help alleviate the unbalanced distribution of the input signal between Q_6 and Q_7 because the output impedance of the tail current source is not sufficiently high [16]. Transistors, Q_{8-9}, are introduced to alleviate the Miller effect so as to enhance bandwidth. A differential CE amplifier with high common mode rejection is used to amplify the desired signal and reduce the phase and amplitude imbalance of the differential signal [17]. An impedance peaking LC network is used as a load of the STD circuit. The high impedance of the LC network is achieved by setting the resonant frequency of the LC network to about 60 GHz. Therefore the gain of the STD circuit can be enhanced. The output 50 Ω impedance matching network included for testing purpose is constructed by placing a series capacitor inductor and capacitor network (CLC) at the output path. Transmission line (T-line) inductors TL_{9-10} in the CLC network are constructed using the top and second metallisation layers. In order to provide better impedance matching, the line-impedance of TL_{9-10} is designed to be 50 Ω at 60 GHz. For accurate simulation, the parasitic

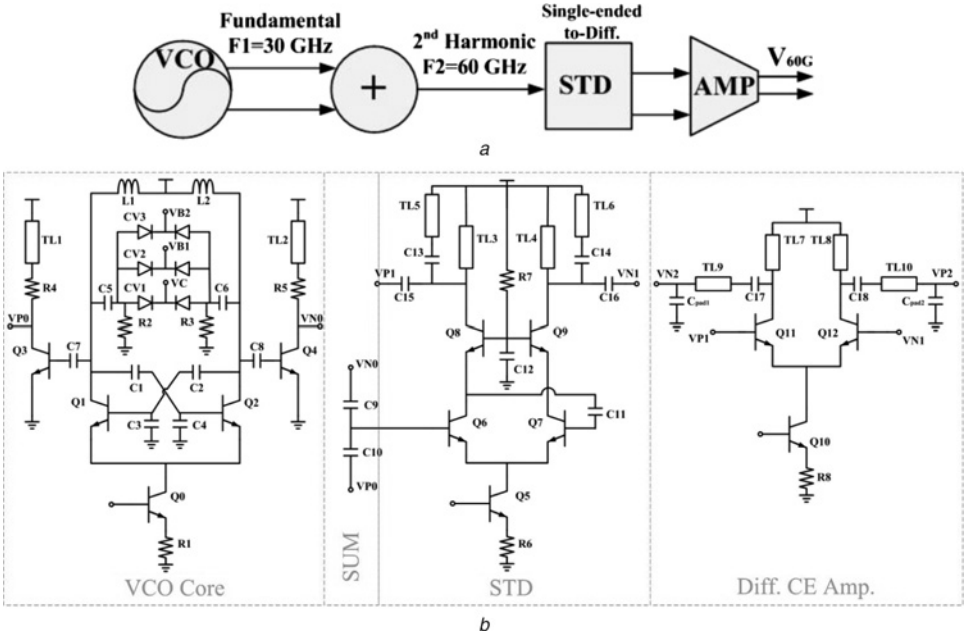

Fig. 1 *Schematic of the proposed wide tuning range VCO*

a Block diagram
b Schematic

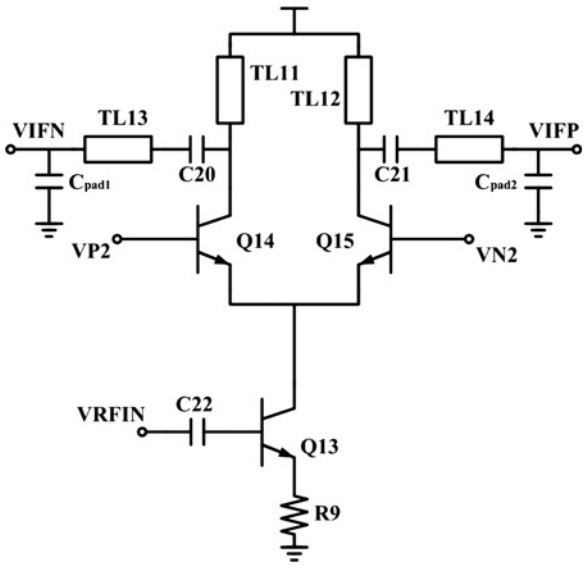

Fig. 2 *Schematic of the single-balanced mixer used to down-convert VCO output signal to low frequency*

capacitance from the I/O pad is also modelled and included in the circuit simulation. All bias networks in the proposed VCO are omitted in the schematic shown in Fig. 1*b*. Resistors are added to the emitter node of tail current sources to increase the output impedance to provide better common mode noise rejection [17]. The transmission line inductors used in the circuit are those available in the standard process design kit.

In order to check the differential phase imbalance of the output differential pair of the proposed VCO, an on-chip single-balanced down-convert mixer is integrated on the same chip as the wideband VCO. The schematic of the mixer is shown in Fig. 2. The two output signals from the VCO shown in Fig. 1 are directly fed into the LO ports of the mixer. In this circuit, the output 50 Ω impedance matching network is removed from the output nodes of the emitter coupled differential amplifier since high output voltage swing is required to switch the transistors on/off in the mixer circuit. Instead, the output impedance matching network is moved to the output path of the down-convert mixer.

Assuming the LO signals from the VCO core are $A_{\rm osc}\cos(\omega_{\rm osc}t)$ and $A_{\rm osc}\cos(\omega_{\rm osc}t+\pi+\Delta\theta)$, respectively. Here, $A_{\rm osc}$ and $\omega_{\rm osc}$ represent the amplitude and frequency of the LO signal, respectively. $\Delta\theta$ stands for the differential phase imbalance between two LO signals. Under the condition of a small signal injection $A_{\rm rf}\cos(\omega_{\rm rf}t)$ at the radio frequency (RF) port, the products at the intermediate frequency (IF) output ports of the mixer are

$$V_{\rm IF1}=\frac{A_{\rm osc}A_{\rm rf}}{2}[\cos(\omega_{\rm osc}-\omega_{\rm rf})t+\cos(\omega_{\rm osc}+\omega_{\rm rf})t] \quad (1)$$

$$V_{\rm IF2}=\frac{A_{\rm osc}A_{\rm rf}}{2}[\cos(\omega_{\rm osc}+\pi+\Delta\theta-\omega_{\rm rf})t+\cos(\omega_{\rm osc}+\pi+\Delta\theta+\omega_{\rm rf})t] \quad (2)$$

where $V_{\rm IF1}$ is the IF signal at one output port of the mixer and $V_{\rm IF2}$ is the IF signal at the other output port. It can be seen obviously from (1) and (2) that the differential phase imbalance between two down/up converted IF signals at mixer output is exactly the same as that between two LO driving signals. By measuring the phase difference between the two IF signals we can learn the phase difference of the VCO outputs.

3 Measurement results

The proposed wideband VCO was fabricated using 0.35 μm SiGe technology. The transit frequency $f_{\rm T}$ of high-speed NPN transistor in the process used is about 170 GHz under an optimal current density 5 mA/μm^2. The microphotograph of the proposed VCO is shown in Fig. 3. The VCO was measured using an Agilent 11974 V preselected millimeter mixer and an Agilent E4407B spectrum analyser. The VCO has four discrete frequency bands which improves the frequency tuning range and decreases the VCO gain. The VCO operates from 58.85 to 70.85 GHz as shown in Fig. 4 with about 20% frequency tuning range. The measured VCO gain for the four frequency bands increases from 0.97 to 1.6 GHz/V. This is because of the decrease of the varactor size. The output power of the VCO ranges from −40 to −35 dBm, as shown in Fig. 5. The measured output power is much lower than the simulated signal power both at VCO core output nodes, which is around −27 dBm, and the entire circuit output nodes, which is around −16 dBm. Therefore through comparing the simulated and measured results some reasons for the low output power can be concluded. The deterioration on the gain of the STD and output buffer stage may be the most

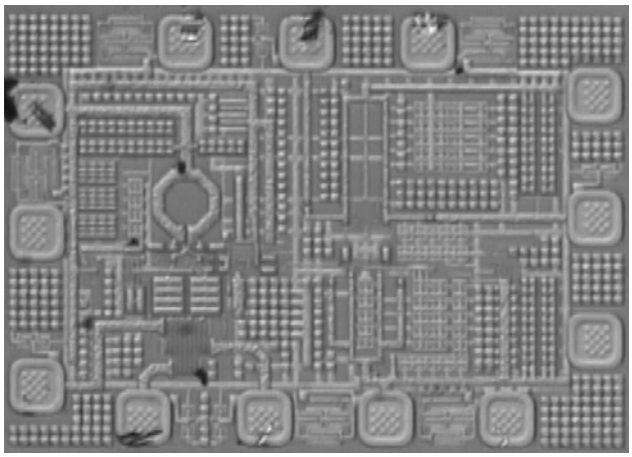

Fig. 3 *Microphotograph of the wide tuning range VCO*

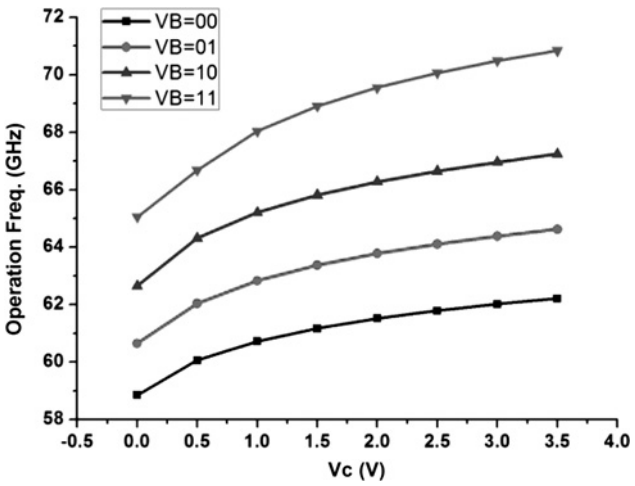

Fig. 4 *Measured oscillation frequency of the wide tuning range VCO*

doi: 10.1049/iet-map.2010.0388

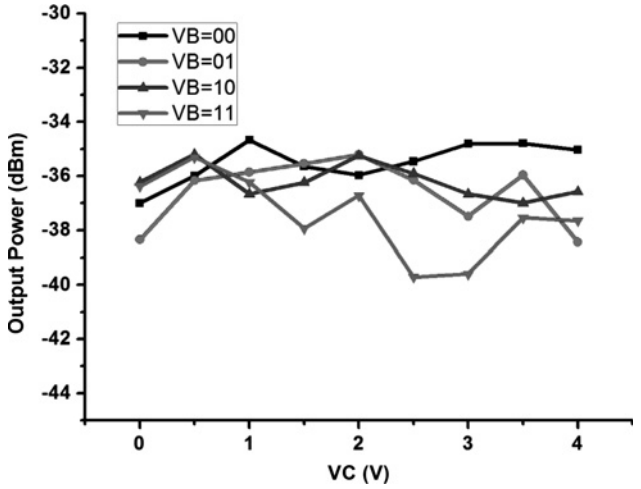

Fig. 5 *Measured output power of the proposed VCO*

important reason for it. The loss of the second harmonic signal power at VCO core output nodes might be another reason causing low output signal power. The measured phase noise at 3 MHz offset, shown in Fig. 6, ranges from −78 to −89.5 dBc/Hz across the entire tuning range, which is measured using following equation

$$P_N = P_\Delta - P_0 - 10_{\log}(\mathrm{RBW}) \tag{3}$$

where P_Δ and P_0 are the measured powers at the offset and central frequencies, respectively. RBW is the resolution bandwidth of the power spectrum analyser and set to 1 MHz during measuring the chips. This relatively high phase noise level is mainly because of the limited Q-factor of the p–n junction varactor bank used in the LC tank and the wide frequency tuning targeted in this design. The phase noise can be improved by increasing the output amplitude and the Q-factor of the varactor bank, or by reducing the frequency tuning range and VCO gain. The output power spectrum at 69.5 GHz is shown in Fig. 7. The entire circuit occupies 770 × 550 μm^2 die area and consumes 62 mA under 3.5 V dc supply. The VCO core, STD and differential CE amplifier consume 37, 11 and 14 mA, respectively. Obviously, about 40% of total power is dissipated by the STD and CE amplifier. The purpose of the high current bias for the VCO core is to achieve large output voltage swing but keeps the VCO operating inside the current limited region. The commonly accepted Figure of Merit considering frequency tuning range ($\mathrm{FoM_T}$) is defined as [4]

$$\mathrm{FoM_T} = \mathrm{PN} - 20_{\log}\left(\frac{f_0}{\Delta_f}\cdot\frac{\mathrm{FTR}}{10}\right) + 10_{\log}\left(\frac{P_{\mathrm{diss}}}{1\,\mathrm{mW}}\right) \tag{4}$$

where PN is the phase noise at an offset frequency Δf from centre frequency f_0. FTR represents the frequency tuning range of the oscillator. P_{diss} is the total power dissipation of the VCO in milli-watts. The measured $\mathrm{FoM_T}$ of the proposed VCO ranges from −150 to −160 across the entire oscillation frequency band. The measurement results of the proposed VCO are summarised in Table 1. Some published

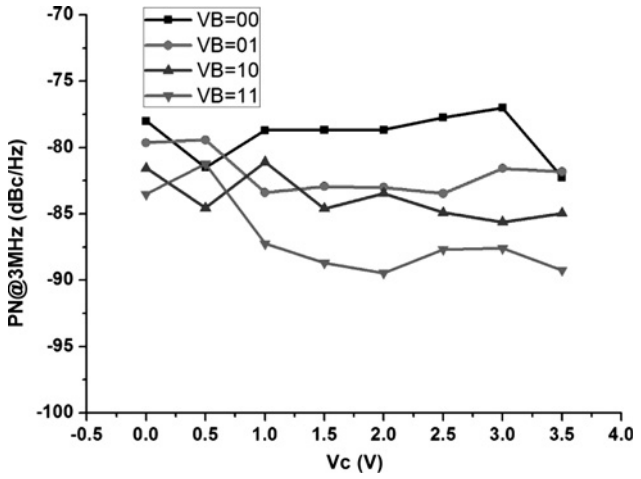

Fig. 6 *Measured phase noise at 3 MHz offset of the wide tuning range VCO*

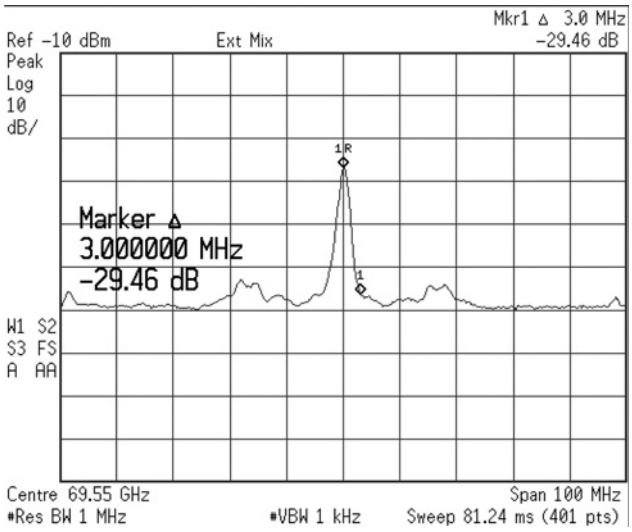

Fig. 7 *Measured output power spectrum at 69.5 GHz*

Table 1 Summary of the measurement results of the proposed VCO and other published VCOs

Ref.	[18]	[19]	[20]	[21]	[22]	[23]	[24]	This work
Tech., μm	0.13 CMOS	0.18 CMOS	0.18 CMOS	0.25 SiGe BiCMOS	0.35 SiGe	0.8 SiGe	0.35 SiGe	0.35 SiGe
Fosc, GHz	62.1	63	69	62.2	80	79	94	60
FTR, %	10	1	5.2	2.0	30	27.8	10.6	20
PN @ 1 MHz, dBc/Hz	−95	−89	−76	−86.1	−97	−83	−86.7[a]	−89.5[a]
Pdiss, mW	3.9	74	27.5	121	240	315.5	185	217
Pout, dBm	−15	−25	−18.5	−28	12	−3.4	−25	−35
$\mathrm{FOM_T}$	−184.8	−146	−152.6	−146.1	−180.8	−164.8	−155	−160

[a]Phase noise was measured at 3 MHz offset

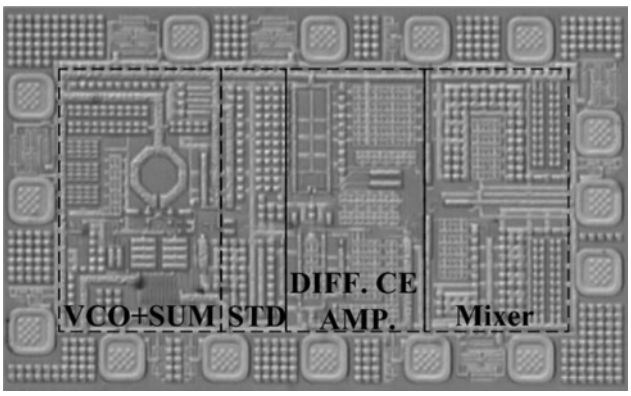

Fig. 8 *Microphotograph of the wideband VCO with down-convert mixer*

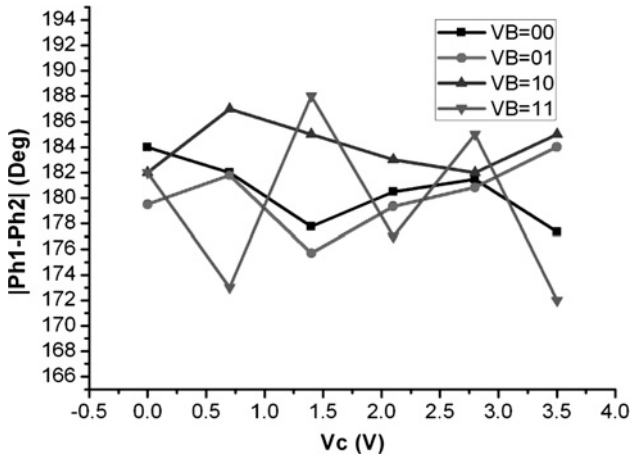

Fig. 9 *Measured differential phase imbalance*

VCOs operating at equivalent frequencies are also listed in the table for comparison.

The microphotograph of the circuit, including the wideband VCO and a down-convert mixer, for differential phase imbalance measurement is shown in Fig. 8. The frequency of the injecting RF signal of the mixer is tuned from 55.8 to 68 GHz to obtain a constant IF frequency at around 3 GHz. The down-converted IF signal was observed using an Agilent 54855A Infiniium Oscilloscope. The measured differential phase imbalance is illustrated in Fig. 9, which shows that the maximum differential phase error is less than 8°. The chip size for the circuit, including VCO and mixer, is 900 × 550 μm^2. The circuit consumes 70 mA under 3.5 V dc supply, of which 8 mA is dissipated by the single-balanced mixer.

4 Conclusions

A wide tuning range low gain VCO consisting of a VCO core, a summing circuit, a STD converter and a differential amplifier, is presented in this paper. The second harmonic signal of the VCO core is extracted by the summing circuit in single-ended form. Then a STD converter is employed to obtain a differential pair. The differential amplifier is designed to have high common mode rejection capability and used as the final stage to improve the phase imbalance of the differential pair. The differential phase error of the output signal is measured by the aid of an on-chip down-convert mixer. The proposed VCO oscillates from 58.85 to 70.85 GHz with about 20% tuning range. The measured phase noise at 3 MHz offset ranges from −78 to −89 dBc/Hz. The gain of the proposed VCO is less than 1.6 GHz/V. The measured differential phase error of the output signal is less than 8°. The VCO dissipates 217 mW.

5 Acknowledgments

The authors would like to thank Infineon Technologies AG for fabricating the chips and its staff members in Infineon Technologies Austria AG for various discussions. In addition the assistance of N. Buchanan in making on-chip measurements is also acknowledged. The work was sponsored by the N. Ireland Department of Education Strengthening all Island Mobile Wireless Futures programme and the 7th Framework Industry–Academia Partnerships and Pathways Programme, Giga Radio.

6 References

1 Standard ECMA-387: 'High rate 60 GHz PHY, MAC and HDMI PAL' (2008, 1st edn.)
2 Rogers, J., Plett, C., Dai, F.: 'Integrated circuit design for high-speed frequency synthesizer' (Artech House, 2006)
3 Dyadyuk, V., Bunton, J., Kendall, R., *et al.*: 'Improved spectral efficiency for a multi-gigabit Mm-wave communication system'. IEEE European Microwave Conf., 2007, pp. 810–813
4 Chien, J.C., Lu, L.H.: 'A 40-GHz wide-tuning-range VCO in 0.18-μm CMOS'. IEEE Symp. on VLSI circuits, 2006
5 Huang, G., Kim, B.-S.: 'Programmable active inductor-based wideband VCO/QVCO design', *IET Microw. Antennas Propag.*, 2008, **2**, (8), pp. 830–838
6 Lu, L.-H., Hsieh, H.-H., Liao, Y.-T.: 'A wide tuning-range CMOS VCO with a differential tunable active inductor', *IEEE Trans. Microw. Theory Tech.*, 2006, **54**, (9), pp. 3462–3468
7 Cho, Y.H., Tsai, M.D., Chang, H.Y., *et al.*: 'A low phase noise 52 GHz push-push VCO in 0.18 μm bulk CMOS technologies'. IEEE RFIC Symp., 2005, pp. 131–134
8 Chiu, H.C., Kao, C.P.: 'A wide tuning range 69 GHz push-push VCO using 0.18 μm CMOS technology', *IEEE Microw. Wirel. Compon. Lett.*, 2010, **20**, (2), pp. 97–99
9 Huang, P.-C., Tsai, M.-D., Vendelin, G.-D.: 'A low-power 114-GHz push-push CMOS VCO using LC source degeneration', *IEEE J. Solid-State Circuits*, 2007, **42**, (6), pp. 1230–1239
10 Chang, C.-C., Liu, R.-C., Wang, H.: 'A 40-GHz push–push VCO using 0.25-μm CMOS technology'. IEEE Asia-Pacific Microwave Conf., December 2003, pp. 73–76
11 Razavi, B.: 'RF microelectronics' (Prentice Hall, 1998)
12 Huang, B.-J., Huang, B.-J., Lin, K.-Y., *et al.*: 'A 20–40 GHz active balun using 0.13 um CMOS process', *IEEE Microw. Wirel. Compon. Lett.*, 2009, **19**, (3), pp. 164–166
13 Costantini, A., Lawrence, B., Mahon, S., *et al.*: 'Broadband active and passive balun circuits: fundamental blocks for modern millimetre-wave radio architectures'. IEEE Proc. EuMA, 2006, pp. 421–424
14 Kral, A., Behbahani, F., Abidi, A.A.: 'RF-CMOS oscillators with switched tuning'. IEEE Proc. Custom Integrated Circuits Conf., May 1998, pp. 555–558
15 Ahn, Y.-G., Kim, S.-K., Chun, J.-H., *et al.*: 'Efficient scalable modeling of double-π equivalent circuit for on-chip spiral inductors', *IEEE Trans. Microw. Theory Tech.*, 2009, **57**, (10), pp. 2289–2300
16 Huang, G., Kim, S.-K., Kim, B.-S.: 'A wideband LNA with active balun for DVB-T application'. IEEE Int. Symp. on Circuits and Systems, 2009, pp. 421–424
17 Gray, P.R., Hurst, P.J., Lewis, S.H., *et al.*: 'Analysis and design of analog integrated circuits' (John Weley & Sons, 2010, 5th edn.)
18 Borremans, J., Dehan, M., Scheir, K., Kuijk, M., Wambacq, P.: 'VCO design for 60 GHz applications using differential shielded inductors in 0.13 μm CMOS'. IEEE Radio Frequency Integrated Circuits Symp., 2008, pp. 135–138
19 Hsieh, H.-H., Lu, L.-H.: 'A 63-GHz Voltage-controlled oscillator in 0.18-μm CMOS'. IEEE Symp. on VLSI Circuits, 2007, pp. 178–179
20 Chiu, H.-C., Kao, C.-P.: 'A wide tuning range 69 GHz push-push VCO using 0.18 um CMOS technology', *IEEE Microw. Wirel. Compon. Lett.*, 2010, **20**, (2), pp. 97–99

21 Veenstra, H., Notten, M.G.M.: '60 GHz VCOs with transmission line resonator in a 0.25 um SiGe BiCMOS technology'. IEEE Radio Frequency Integrated Circuits Symp., 2008, pp. 119–122
22 Pohl, N., Rein, H.-M., Musch, T., Auginger, K., Hausner, J.: 'SiGe bipolar VCO with ultra-wide tuning range at 80 GHz center frequency', *IEEE J. Solid-State Circuits*, 2009, **44**, (10), pp. 2655–2662
23 Gang, L., Ulusoy, A., Trasser, A., Schumacher, H.: '64 to 86 GHz VCO utilizing push-push frequency doubling in a 80 GHz f_T SiGe HBT technology'. Topical Meeting on IEEE Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2010, pp. 239–242
24 Huang, G., Fusco, V.: 'A 94 GHz wide tuning range SiGe bipolar VCO using a self-mixing technique', *IEEE Microw. Wirel. Compon. Lett.*, 2011, **21**, (2), pp. 86–88